



OK301

USB

键盘加密控制器

规格书

Version 1.1

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奥乐科技股份有限公司
oTHE Technology Inc.
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1. 简介

OK301 是一个用在标准 USB 键盘的加密控制器。其内部包含 USB 键盘扫描控制器，及经美国 NIST FIPS 认证的 AES 加密引擎，透过 OK301 组合成的 USB 键盘与软件端的加密整合技术，可以主动防治网络黑客或键盘侧录软件等的恶意盗取个人信息，解决用户在上网时的疑虑，及被侧录的情况发生。

OK301 内含奥乐科技自行研发的 8-Bit RISC CPU、加密运算器及 8K Bytes Flash，它提供 USB V2.0 的接口与 V1.1 的通讯协议，同时整合了传统的键盘扫描电路、自动侦测电路及鬼键消除电路，更可以接受同一时间按下 12 个键，解决传统 USB 键盘无法同一时间按下超过 6 个键的限制。OK301 特殊的电源管理机制，让 USB 键盘运作的功耗降到最低，不仅可用于传统桌面计算机键盘，也适用于笔记本电脑键盘。

OK301 采用标准的 LQFP-48Pin 封装，针对黑客及键盘侧录软件等恶意盗取个人信息的情况，OK301 是一个同时可以做到低成本、高安全性与实用性的 USB 加密键盘保护方案。

2. 功能

- 单指令 RISC 架构 (TSIR) 的 8-Bit MCU
- 内建 256 Bytes SRAM 与 8KB Flash
- USB 2.0 接口 low speed 及 V1.1 协议
- 支持两组 SPI 接口
- 支持 8 x 18 键盘扫描矩阵
- 内建自动键盘扫描侦测及鬼键消除电路
- 支持同一时间按下 12 个键
- 键盘扫描侦测无 Buffer 限制
- 内建 AES 加密引擎 (US NIST FIPS 认证#1576)
- 支援 Windows 98/ 2000/ NT/ XP/ Vista/ 7
- 支持多媒体及特殊编码键盘
- 内建提升电阻
- 支持碳膜键盘
- 内建电源管理及看门狗电路
- 内建低功耗振荡器
- 内建 3.3V 电压调整器
- 工作电压: 4.5~5.5V
- 封装: LQFP-48 pin

3. 内部方块图

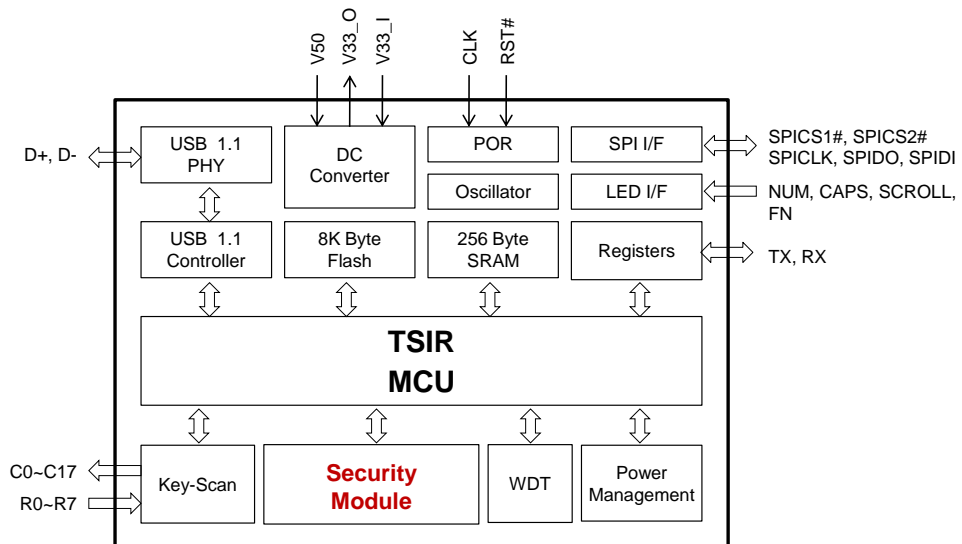


图 3-1: OK301 内部方块图

4. 脚位图

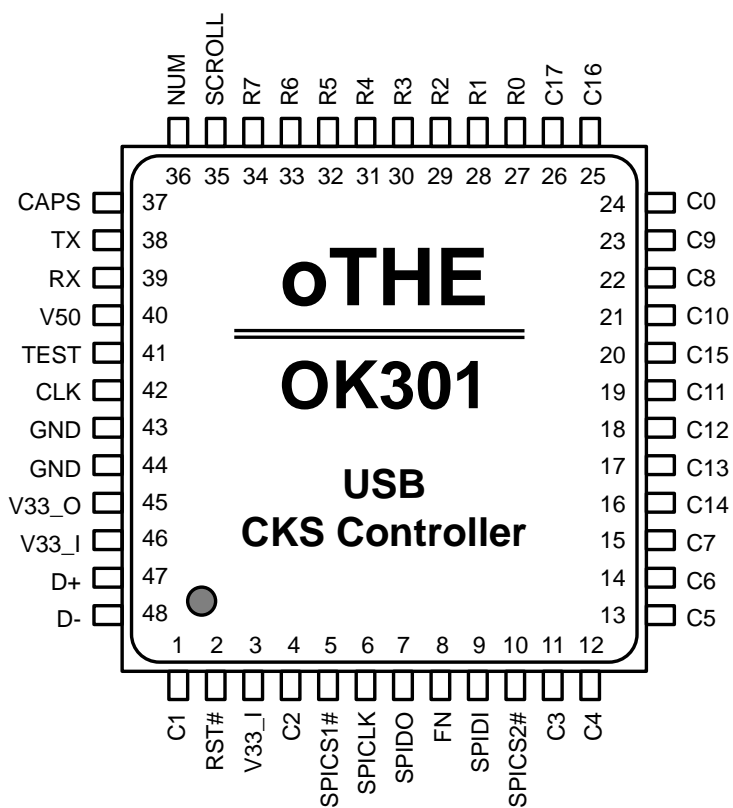


图 4-1: OK301-LQ48 (LQFP-48pin)

5. 产品编号

表 5-1: 产品编号

产品编号	封装规格
OK301-LQ48	LQFP-48pin

6. 脚位定义

表 6-1: 脚位定义

脚位名称	I/O	说 明
R0~R7	I	Keyboard Scan Input
C0~C17	O	Keyboard Scan Output
SPICS1#	O	SPI Master Chip Select 1
SPICS2#	O	SPI Master Chip Select 2
SPICLK	O	SPI Master Clock Output
SPIDO	O	SPI Master Data Output
SPIDI	I	SPI Master Data Input
SCROLL	O	Scroll lock LED
NUM	O	Num Lock LED
CAPS	O	Caps Lock LED
FN	O	Fn Lock LED
TX	O	UART TX
RX	I	UART RX
D+	I/O	USB PHY I/F D+
D-	I/O	USB PHY I/F D-
CLK	I	External CLK (optional)
RST#	I	External Reset (optional)
TEST	I/O	Test Pin
V50	PWR	5V Power from USB Connector
V33_O	PWR	3.3V Regulator Output
V33_I	PWR	3.3V Regulator Input (2.0V~3.3V)
GND	PWR	Power Ground

7. 功能说明

7-1 键盘矩阵

表 7-1: 键盘矩阵对照表

	R0	R1	R2	R3	R4	R5	R6	R7
C0	Pause	Power	€	Sleep	Ctrl-R	Wake-up	Ctrl-L	F5
C1	Q	Tab	A	ESC	Z	N-CHG	` (~)	1 (!)
C2	W	CAP	S	K45	X	CHG	F1	2 (@)
C3	E	F3	D	F4	C	ROMA	F2	3 (#)
C4	R	T	F	G	V	B	5 (%)	4 (\$)
C5	U	Y	J	H	M	N	6 (^)	7 (&)
C6	I] (})	K	F6	, (<)	K56	= (+)	8 (*)
C7	O	F7	L	¥	. (>)	APP	F8	9 ('')
C8	P	[({)	; (:)	' (")	K42	/ (?)	_ (-)	0 ('')
C9	Scroll		Fn	Alt-L	M/Mode	Alt-R		Print Scr
C10	K14	Back	\ ()	F11	Enter-L	F12	F9	F10
C11	7 (Home)	4 (←)	1 (End)	Space	Num	↓	Del	Power
C12	8 (↑)	5	2 (↓)	0 (Ins)	/	→	Ins	Sleep
C13	9 (PgUp)	6 (→)	3 (PgDn)	. (Del)	*	-	Page Up	Page Dn
C14	+	K107	Enter-R	↑	Paly/Pause	←	Home	End
C15	Wake Up	Shift-L	Shift-R	Volume -	Volume +	NextTrack	PrevTrack	Media
C16	Mail	Win-L	WWW Forward	WWW Stop	WWW Back	WWW Refresh	Mute	WWW Search
C17	KC-L	WWW Favorites	Win-R	My Computer	Stop	Caculator	Web/Home	KC-R

8. 电气特性

8-1 最大极限

表 8-1:最大极限值

说 明	符 号	数 值	单 位
Supply Voltage on V50 Relative to GND	V_{DD}	-0.5V~+6.5V	V
Supply Voltage on V33_I Relative to GND	V_{33_I}	-0.5V~+4.0V	V
Input Voltage Range	V_{IN}	-0.3 to $V_{DD}+0.3$	V
Power Dissipation	P_D	≤ 300	mW
Operation Temperature Range	T_{OPR}	-0 to +70	°C
Storage Temperature	T_{ST}	-45 to +150	°C
Soldering Temperature (10 seconds, Note 2)	T_{SOLDER}	260	°C

Notes:

1. These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.
2. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heat stress the package.
3. All supply voltages are referenced to GND = 0V.

8-2 DC 特性

表 8-2: DC 特性

符号	说明	条件	Min.	Typ.	Max.	单位
V ₅₀	Supply Power	USB 5V	4.5	5	5.5	V
V _{IH1}	R0~R7 Input High	Voltage Schmitt-trigger is built-in	1.9		VDD+0.3	V
V _{IL1}	R0~R7 Input Low	Voltage Schmitt-trigger is built-in	-0.3		1.6	V
V _{IH2}	Input High	Voltage Schmitt-trigger is built-in	2.4		VDD+0.3	V
V _{IL2}	Input Low	Voltage Schmitt-trigger is built-in	-0.3		1.7	V
V _{OH}	Output High	Voltage I _{OH} = -2mA		V33_I - 0.3		V
V _{OL}	Output Low	Voltage I _{OL} = 2mA		0		V
I _{DS}	Drive/Sink Current for LED	V _{OL} = 0.2V (R=220 ohm)		8		mA
I _{IN}	Input Leakage Current	V33_I = 3.3V	-1		1	μA
R _{P1}	Pull up Resistance		60	80	100	KΩ
R _{P2}	Pull up Resistance	For Carbon wire	1.5	1.8	2.1	MΩ
I _{OP1}	Chip Operating Current	USB connected, continuous key pressed		2		mA
I _{OP2}	Chip Operating Current	USB connected,		2		mA
I _{SB1}	Chip Standby Current	USB Connected. Int OSC disable		2		mA
I _{SB2}	Chip Standby Current	non-WDT standby		270		μA
V _{33_O}	3.3V Regulator Output	VDD= 5V, 30mA (100Ω load)	3	3.3	3.6	V
F _{OSC}	System Clock	V33_I=3.3V, USB connected.	-1.5%	1.5	+1.5%	MHz
PWR_OK			2	2.05	2.1	V
USB Interface						
V _{ON}	Static Output High	15K ± 5% Ohm to GND	2.8		3.6	V
V _{OFF}	Static Output Low	RUP is enabled			0.3	V
V _{DI}	Differential Input Sensitivity		0.2			V
V _{CM}	Differential Input Common Mode Range		0.8		2.5	V
V _{SE}	Single Ended Receiver Threshold		0.8		2	V
C _{IN}	Transceiver Capacitance				20	pF
I _{IO}	Hi-Z State Data Line Leakage	0V < V _{IN} < 3.3V	-10		10	mA

8-3 AC 特性

表 8-3: AC 特性

符号	说明	条件	Min.	Typ.	Max.	单位
USB Driver						
T_{R1}	Transition Rise Time	CLOAD = 200 pF	75			ns
T_{R2}	Transition Rise Time	CLOAD = 600 pF			300	ns
T_{F1}	Transition Fall Time	CLOAD = 200 pF	75			ns
T_{F2}	Transition Fall Time	CLOAD = 600 pF			300	ns
T_R	Rise/Fall Time Matching		80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
USB Data Timing						
T_{DRATE}	Low-speed Data Rate	Ave. Bit Rate (1.5 Mbps \pm 1.5%)	1.4775		1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	-75		75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	-45		45	ns
T_{DEOP}	Differential to EOP Transition Skew		-40		100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP			330	ns
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675			ns
T_{EOPT}	Source EOP Width		1.25		1.5	μ s
T_{EOPT}	Source EOP Width		1.25		1.5	μ s
T_{UDJ1}	Differential Driver Jitter	To next transition	-95		95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	-95		95	ns
T_{LST}	Width of SE0 during Diff. Transition				210	ns

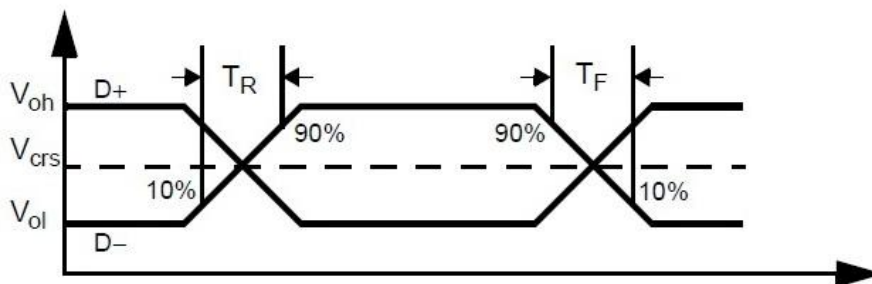
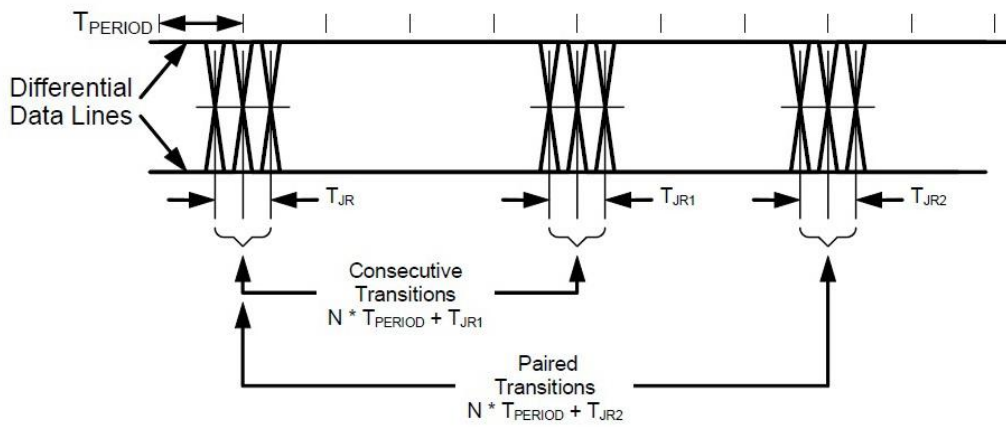
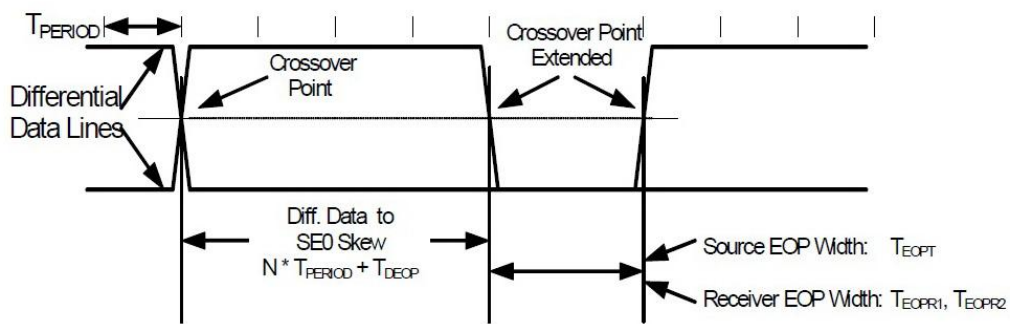
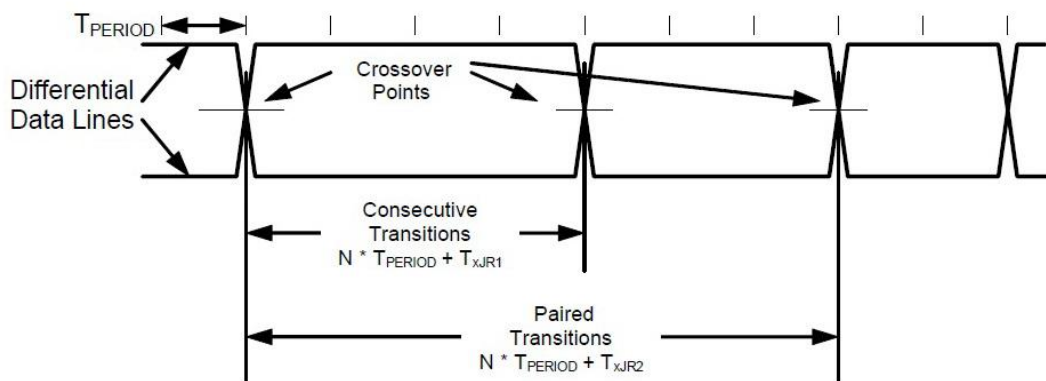


图 8-1: USB Data Signal Timing


图 8-2: Receiver Jitter Tolerance

图 8-3: Differential to EOP Transition Skew and EOP Width

图 8-4: Differential Data Jitter

9. 封装

9-1 LQFP-48 Pin

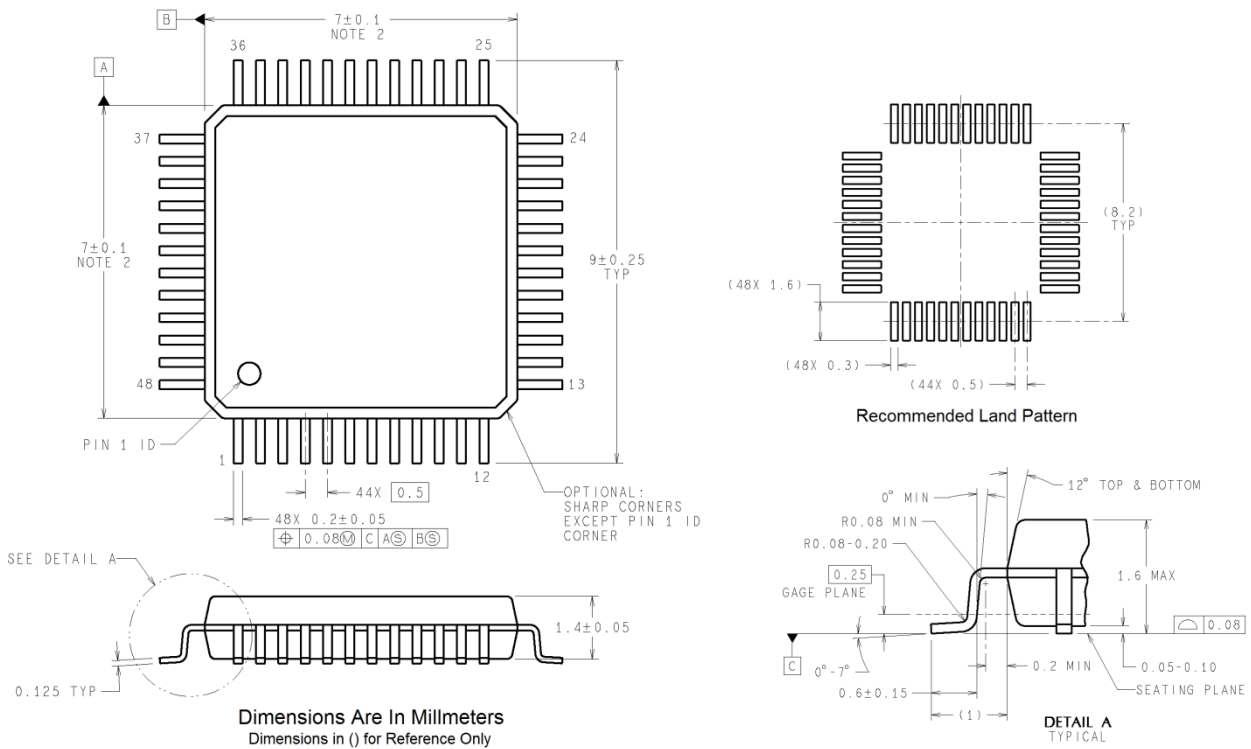


图 9-1: LQFP-48 Pin 封装尺寸

Notes:

1. Dimension does not include mold protrusion. Maximum allowable mold protrusion is 0.25mm per-side.
2. Reference JEDEC registration MS-026, variation BBC.

10. 应用电路

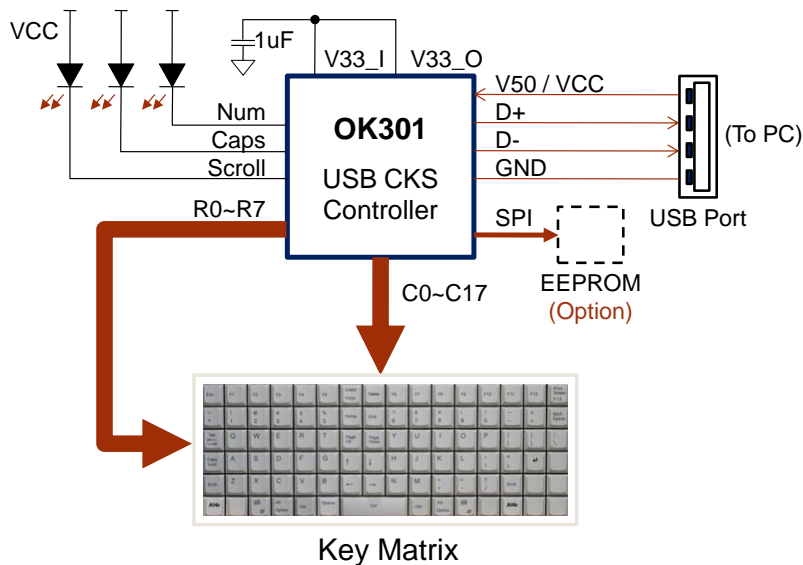


图 10-1: 应用方块图

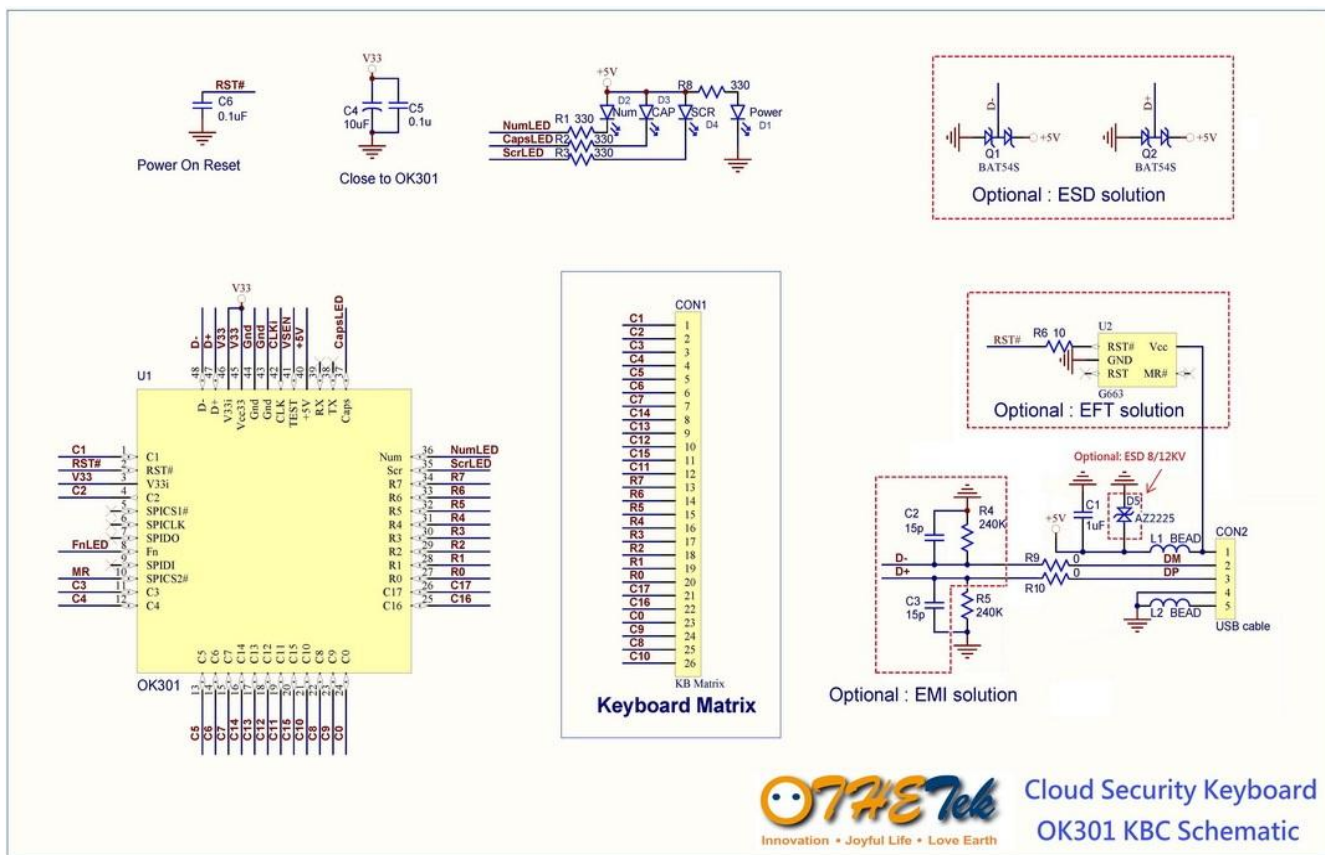


图 10-2: USB 键盘应用电路

表 10-1: USB 键盘零件表

Q'ty	Part Type	Footprint	Description	Designator				
2	0Ω	RES 0603	0Ω SMD Resistor 0603±5%	R9	R10			
3	330Ω	RES 0603	330Ω SMD Resistor 0603±5%	R1	R2	R3	R8	
1	240KΩ	RES 0603	240KΩ SMD Resistor 0603±5%	R5				
2	0.1uF	CAP NPO 0603	0.1uF Capacitor 0603 NPO 50V	C5	C6			
1	1uF	CAP NPO 0603	1uF Capacitor 0603 NPO 50V	C1				
1	10uF	CAP NPO 0805	10uF Capacitor 0805 NPO 50V	C4				
2	FB 300	FB 300 Ω	Ferrite Bead 300Ω @ 100MHz 0805	L1	L2			
4	LED		Power, Num, Cap, Scr	D1	D2	D3	D4	
1	OK301	LQFP 48L	OK301 CKS Chip LQFP48L	U1				
EMI Options								
2	15P	CAP NPO 0603	15pF Capacitor 0603 NPO 50V	C2	C3			
1	240K	RES 0603	240KΩ SMD Resistor 0603±5%	R4				
ESD Options								
2	BAT54S			Q1	Q2			
1	AZ2225		(for ESD 8/12KV)	D5				
EFT Options								
1	10Ω	RES 0603	10Ω SMD Resistor 0603±5%	R6				
1	G663	SOT-23-5	Reset chip	U2				

Note: C5, C6, R1 are for EFT options.

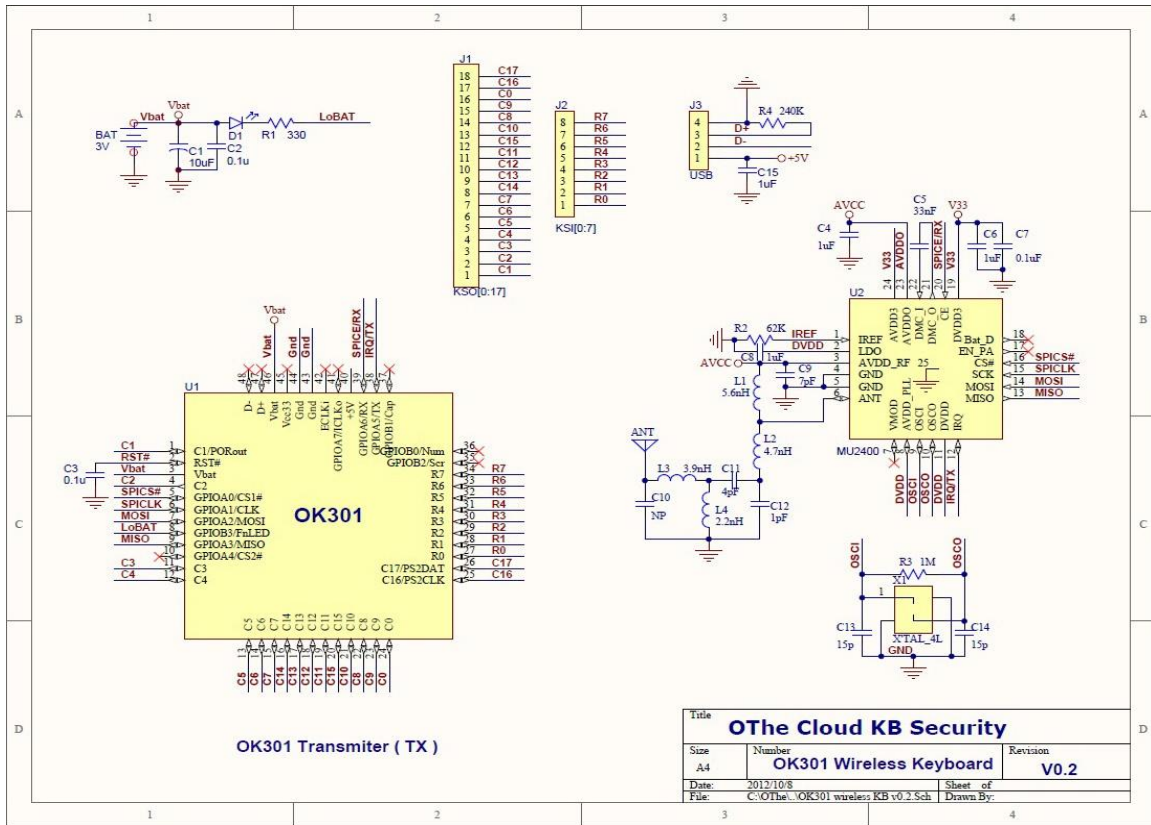


图 10-3 : RF 键盘(发送端)应用电路

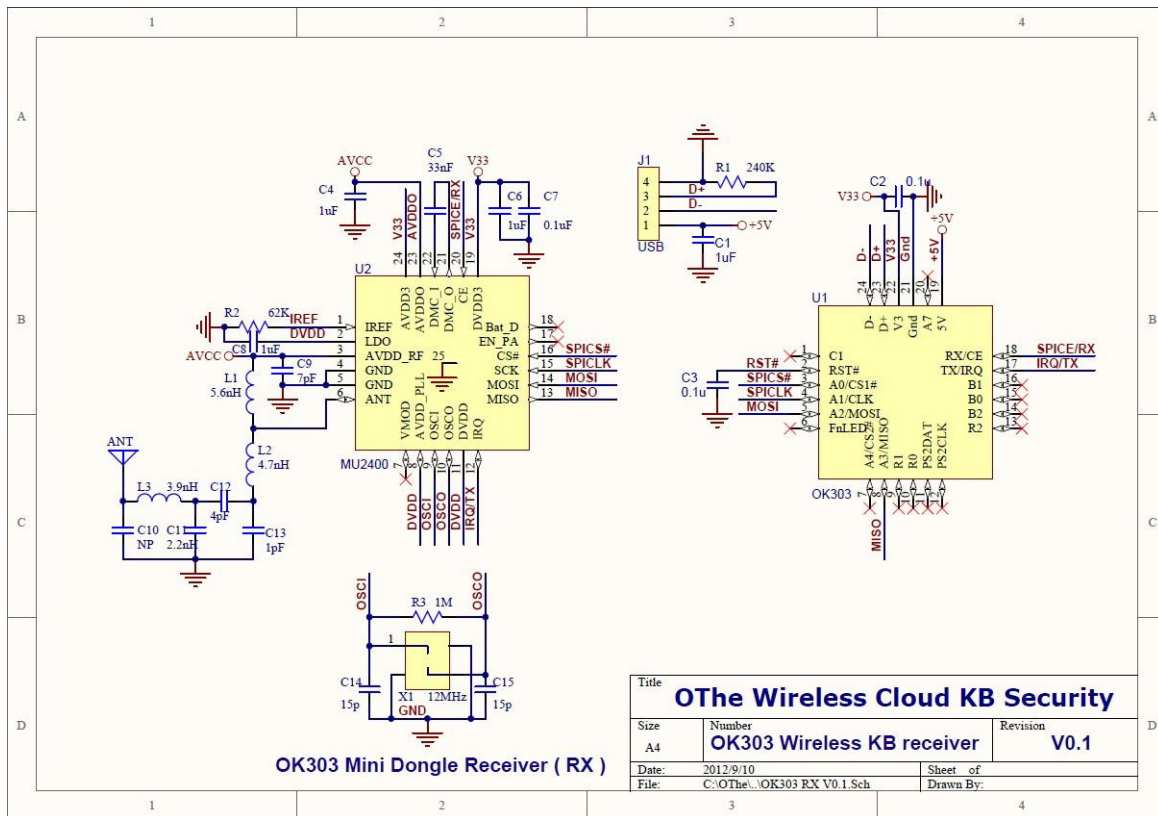


图 10-4 : RF 键盘(接收端)应用电路

About oTHE

oTHE Technology Inc. was founded on August of 2008 located in Hsinchu City, Taiwan by over 15 years experienced RD and Marketing team from Hsinchu Science Park. oTHE team had successful experience and related background specialized in the field of PC related chips. oTHE is a leading and professional IC design company which decided to provide high quality, high performance and high value products and services. oTHE has extensive experience developing computer industry component, especially in PC keyboard controller, keyboard security, security information system and optics.

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奥乐科技股份有限公司

OTHE TECHNOLOGY INC.

30076 新竹市科学园区新安路 5 号 4 楼
4F., No.5, Xin'an Rd., Science Park., Hsinchu City 30076, Taiwan
Tel: +886-666-8690
<http://www.othe.com.tw>