OK103

键盘加密控制器

规 格 书

Version 1.0

August 12, 2011

oTHE Technology Inc.

版 本 更 新 记 录		
版 本	日 期	说 明
1.0	August 12, 2011	Preliminary version

Chapter Contents Page

1. 简介

OK103 是一个用在 2.4G 无线键盘的加密控制器。其内部包含经美国 NIST FIPS 认证的 AES 加密引擎，透过 OK103 组合成的无线键盘与软件端的加密整合技术，可以主动防治网络黑客或键盘侧录软件等的恶意盗取个人信息，解决用户在上网时的疑虑，及被侧录的情况发生。

OK103 内含奥乐科技自行研发的 8-Bit MCU、加密运算器及 8K Bytes Flash，它提供 USB V2.0 的接口与 V1.1 的通讯协议，OK103 是一 SOIC-16Pin 的封装，用在标准个人计算机的 2.4G RF 无线键盘的 Dongle 接收器(Host 端)，对键盘制造商而言，OK103 可以应用在现有的 2.4G RF 无线键盘，甚至不需要修改键盘本体(Device 端)的软硬件及外观，是一个同时可以做到低成本、高安全性与实用性的无线键盘加密保护方案。

2. 功能

- 内建 8-Bit MCU 及硬件加密运算器
- USB 2.0 界面 low speed 及 V1.1 协议
- 内建 256 Bytes SRAM 与 8KB Flash
- 内建 AES 加密引擎 (US NIST FIPS 认证 #1576)
- 提供 SPI 与 GPIO 接口
- 内建 3.3V 电压调整器
- 内建 12 MHz 振荡器
- 3/5V I/O 内建提升电阻
- 工作温度: 0~70°C
- 供应电压 : 4.5~5.5V
- 封装: SOIC-16 pin

3. 内部方块图

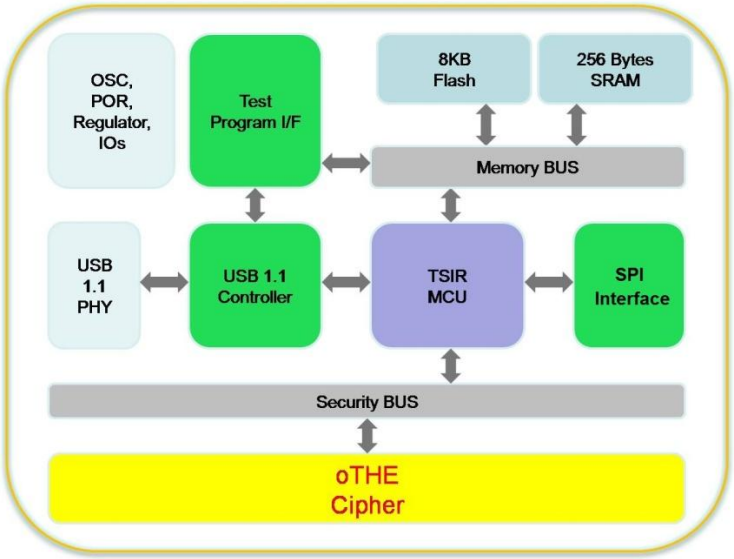

图 3-1：内部方块图

4. 脚位图

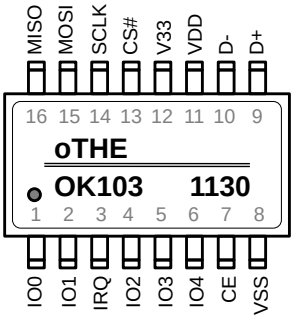

图 4-1 : 脚位图

5. 脚位定义

表 5-1 : 脚位定义

Pin No.	脚 位 名 称	说　　明	Pin state
1,2,4,5,6	IO[4:0]	General Purpose I/O Pins	Bi-direction
3	IRQ	Interrupt request pin.	Input
7	CE	Chip Enable Activates RX or TX mode	Output
8	VSS	Power Ground	Power
9	D-	USB I/F D-	USB PHY
10	D+	USB I/F D+	USB PHY
11	VDD	Power Supply	Power
12	V33	Regulator Output	Power
13	CS#	SPI Chip Select	Output
14	SCLK	SPI Clock	Output
15	MOSI	SPI Data Output	Output
16	MISO	SPI Data Input	Input

6. 封装

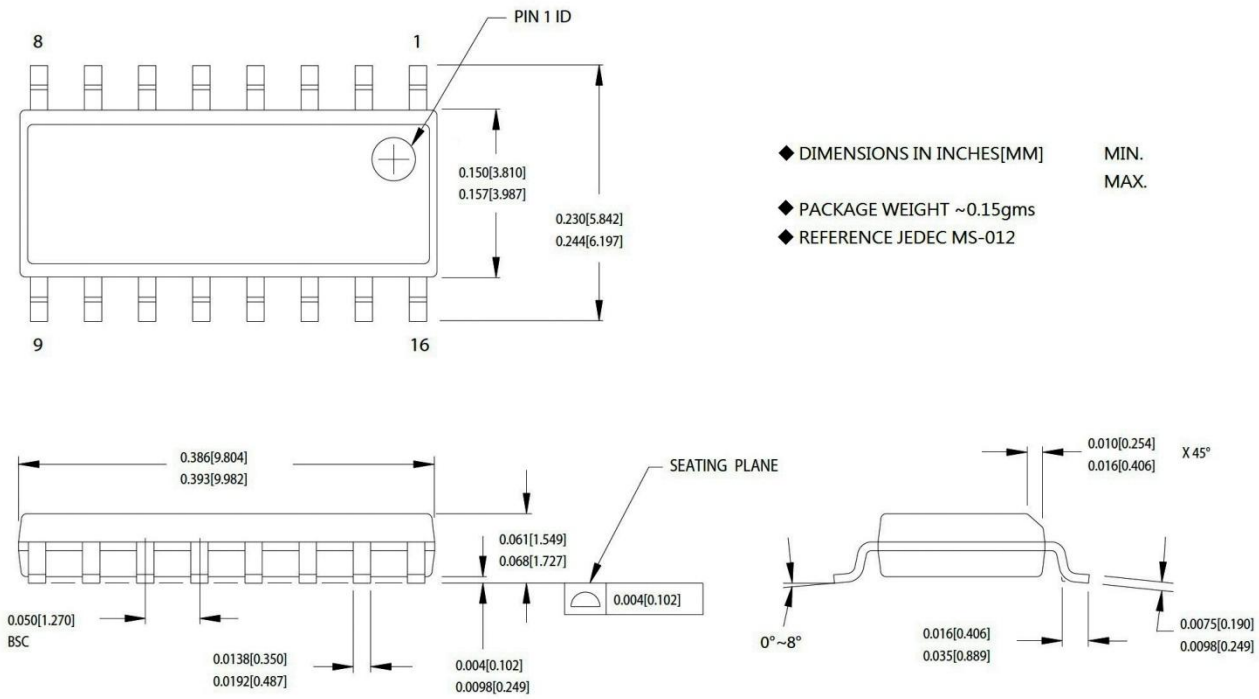

图 6-1 : 16-Lead (150-Mil) SOIC

7. 电气特性

7-1 最大极限

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –0°C to +70°C

Supply Voltage on VDD Relative to VSS..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to + VCC + 0.5V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to + VCC + 0.5V

Power Dissipation ..... 300 mW

Static Discharge Voltage 2200V

Latch-up Current ..... 200 mA

7-2 DC 特性

表 7-1 : DC 特性

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
	General					
V_{DD}	Operating Voltage	USB activity, 12 MHz	4.35		5.25	V
V_{33}	Regulator Voltage	USB activity, 12 MHz		3.3		V
T_{FP}	Operating Temp	Flash Programming	0		70	°C
I_{CC2}	VDD Operating Supply Current	VDD = 5.0V, no loading, 12 MHz		15		mA
I_{SB1}	Standby Current	Internal Oscillators, Bandgap, Flash, CPU Clock, Timer Clock, USB Clock all disabled			10	µA
USB Interface						
V_{ON}	Static Output High	15K ± 5% Ohm to VSS	2.8		3.6	V
V_{OFF}	Static Output Low	RUP is enabled			0.3	V
V_{DI}	Differential Input Sensitivity		0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2	V
C_{IN}	Transceiver Capacitance				20	pF
I_{IO}	Hi-Z State Data Line Leakage	0V < VIN < 3.3V	-10		10	mA

(Continued)

Parameter	Description General	Conditions	Min	Typ.	Max.	Unit
SPI / GPIO Interface						
R_{UP}	Pull up Resistance		4		12	KΩ
V_{ICR}	Input Threshold Voltage Low, CMOS mode	Low to High edge	40%		65%	VDD
V_{ICF}	Input Threshold Voltage Low, CMOS mode	High to Low edge	30%		55%	VDD
V_{ILTTL}	Input Low Voltage, TTL Mode	I/O-pin Supply = 2.9–3.6V			0.8	V
V_{IHTTL}	Input High Voltage, TTL Mode	I/O-pin Supply = 4.0–5.5V	2			V
V_{OL}	Output Low Voltage	IOL2 = 8 mA			0.4	V
V_{OH}	Output High Voltage	IOH = 2 mA	VDD – 0.5			V
C_{LOAD}	Maximum load capacitance				50	pF

7-3 AC 特性

表 7-2：AC 特性

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Driver						
T_{R1}	Transition Rise Time	CLOAD = 200 pF	75			ns
T_{R2}	Transition Rise Time	CLOAD = 600 pF			300	ns
T_{F1}	Transition Fall Time	CLOAD = 200 pF	75			ns
T_{F2}	Transition Fall Time	CLOAD = 600 pF			300	ns
T_R	Rise/Fall Time Matching		80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
USB Data Timing						
T_{DRATE}	Low-speed Data Rate	Ave. Bit Rate (1.5 Mbps ± 1.5%)	1.4775		1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	-75		75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	-45		45	ns
T_{DEOP}	Differential to EOP Transition Skew		-40		100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP			330	ns
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675			ns
T_{EOPT}	Source EOP Width		1.25		1.5	μs
T_{EOPT}	Source EOP Width		1.25		1.5	μs
T_{UDJ1}	Differential Driver Jitter	To next transition	-95		95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	-95		95	ns
T_{LST}	Width of SE0 during Diff. Transition				210	ns
SPI / GPIO Interface						
T_{R_SPI}	Output Rise Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			50	ns
T_{F_SPI}	Output Fall Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			15	ns

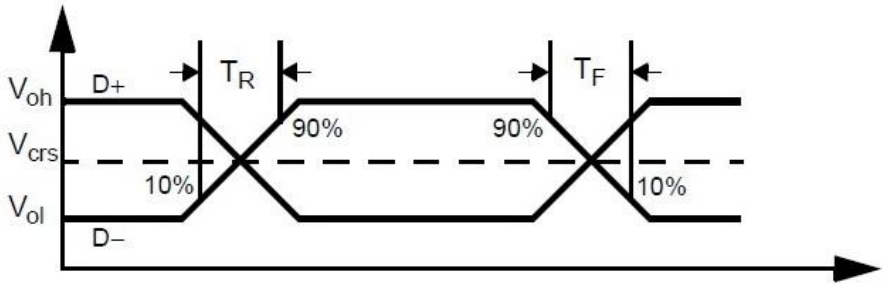

图 7-1 : USB Data Signal Timing

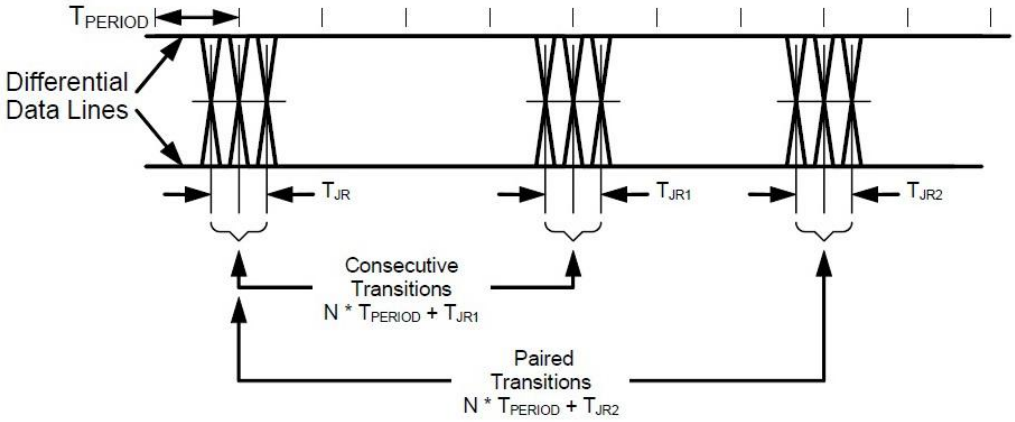

图 7-2 : Receiver Jitter Tolerance

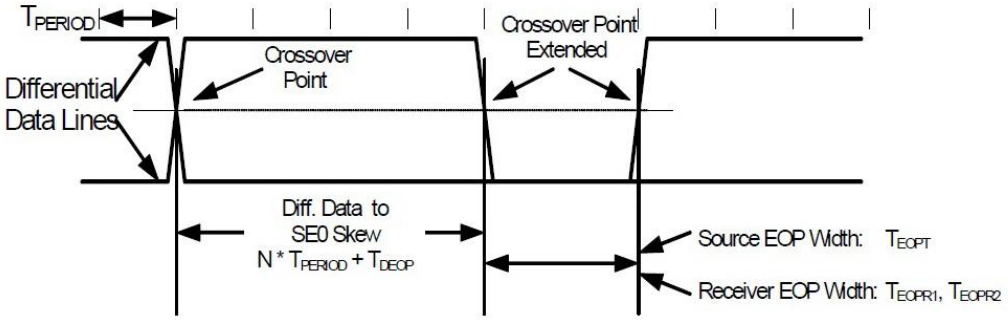

图 7-3 : Differential to EOP Transition Skew and EOP Width

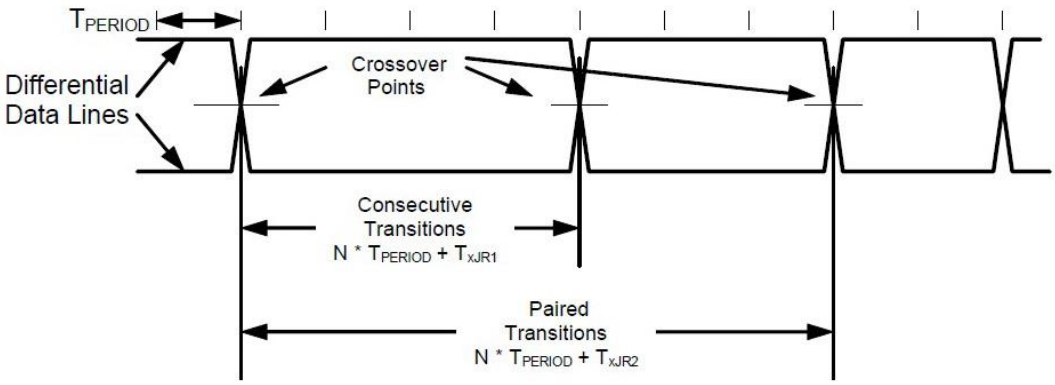

图 7-4 : Differential Data Jitter

8. 应用电路

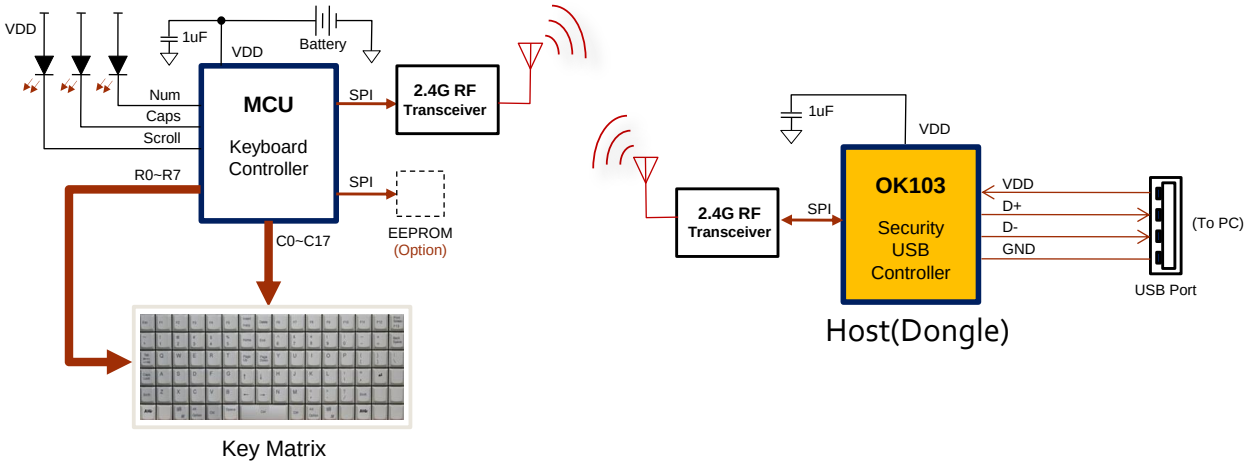

图 8-1：应用电路方块图

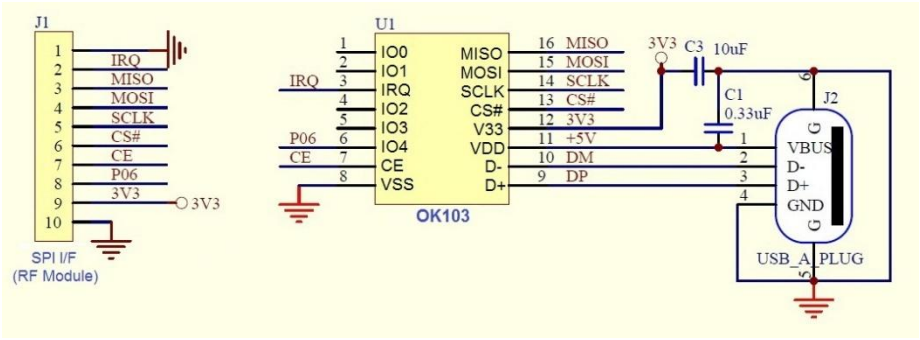

图 8-2：应用电路方块图

图 8-3：应用领域