OK103

Keyboard

Security Controller

Specification

Version 1.0

August 10, 2011

oTHE Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	August 10, 2010	Preliminary version

Chapter Contents Page

1. General Description

The OK103 is a Cloud Keyboard Security(CKS) Controller for 2.4G RF Keyboard/Mouse dongle. Cloud Keyboard Security is a method to resist keylogger for the Personal Computer in the Cloud Computing Internet. The OK103 embedded FIPS certificated AES engine for CKS. By the method of OK103 CKS controller, the keylogger can't steal user's keystrokes with right meanings, so that the online applications are safe for any critical business transaction.

The OK103 built in an oTHE 8-bit single instruction RISC CPU with 8KByte Flash only. It provides USB 2.0 interface and supports USB 1.1 protocol. The OK103 supports SOIC-16Pin package for standard 2.4G keyboard dongle. It is very easy to integrate into existing normal 2.4G RF keyboard, even does not need modify the firmware of Device(Keyboard).

2. Features

- Embedded 8bit MCU and H/W Encrypter
- Embedded 256 Bytes RAM, 8Kbytes Flash
- USB V2.0 low speed and V1.1 protocol
- AES security engine (US NIST FIPS certificated #1576)
- Provide SPI and GPIO Interface
- Embedded 3.3V Regulator
- Internal 12 MHz Oscillator
- 3/5V I/O with Pull-up Resistor
- Operating Temperature: 0~70°C
- Operating Voltage : 4.5~5.5V
- Package: SOIC-16 pin

3. Pin Configuration

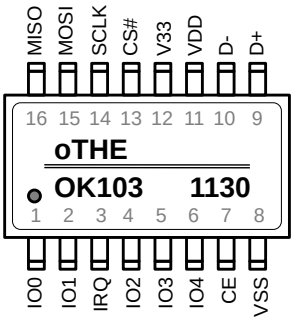

Figure 3-1 : Pin Assignment

4. Block Diagram

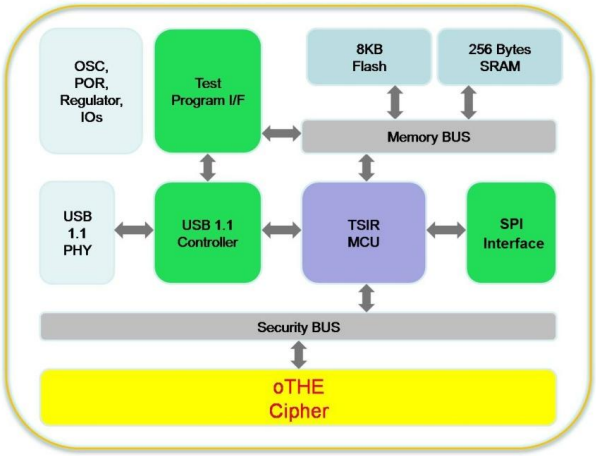

Figure 4-1 : Internal Block Diagram

5. Pin Description

Table 5-1 : Pin Description

Pin No.	Pin Name	Description	Pin state
1,2,4,5,6	IO[4:0]	General Purpose I/O Pins	Bi-direction
3	IRQ	Interrupt request pin.	Input
7	CE	Chip Enable Activates RX or TX mode	Output
8	VSS	Power Ground	Power
9	D-	USB I/F D-	USB PHY
10	D+	USB I/F D+	USB PHY
11	VDD	Power Supply	Power
12	V33	Regulator Output	Power
13	CS#	SPI Chip Select	Output
14	SCLK	SPI Clock	Output
15	MOSI	SPI Data Output	Output
16	MISO	SPI Data Input	Input

6. Package Dimensions

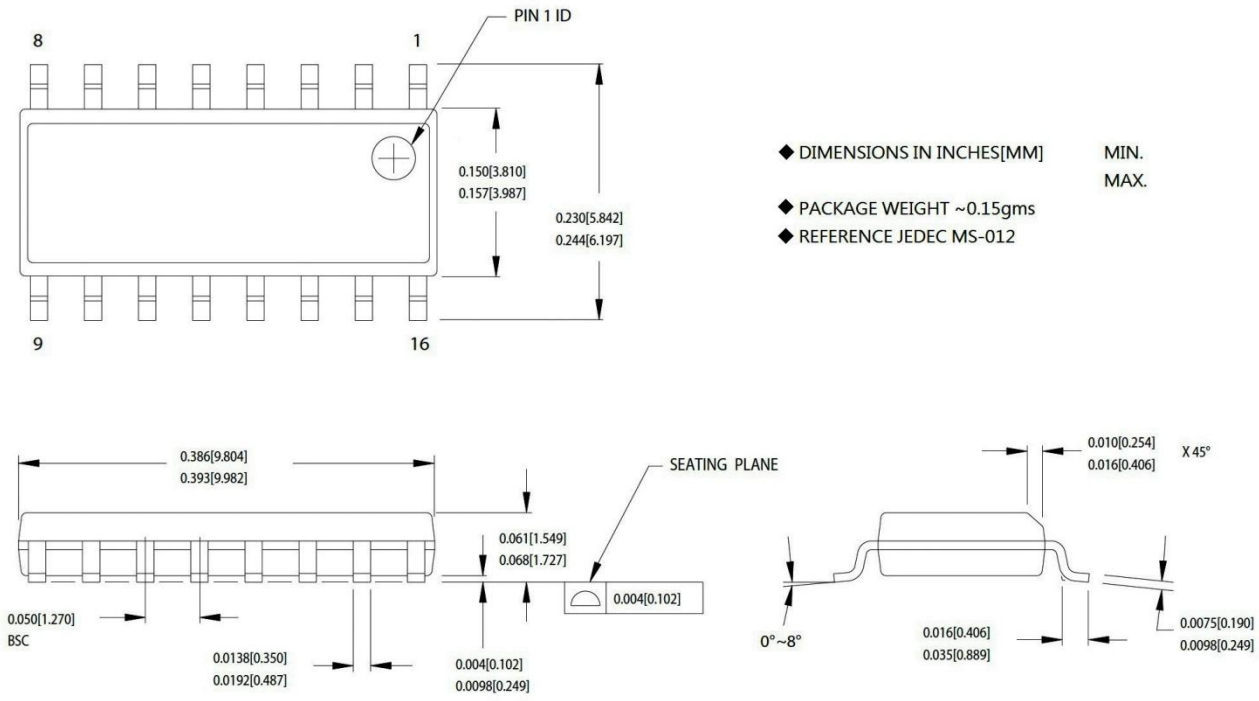

Figure 6-1 : 16-Lead (150-Mil) SOIC

7. Electrical Characteristics

7-1 Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
Supply Voltage on VDD Relative to VSS	–0.5V to +7.0V
DC Input Voltage	–0.5V to + VDD + 0.5V
DC Voltage Applied to Outputs in High-Z State	–0.5V to + VDD + 0.5V
Power Dissipation	300 mW
Static Discharge Voltage	2200V
Latch-up Current	200 mA

7-2 DC Characteristics

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
	General					
V_{DD}	Operating Voltage	USB activity, 12 MHz	4.35		5.25	V
V_{33}	Regulator Voltage	USB activity, 12 MHz		3.3		V
T_{FP}	Operating Temp	Flash Programming	0		70	°C
I_{CC1}	VDD Operating Supply Current	VDD = 5.25V, no loading, 12 MHz			30	mA
I_{CC2}	VDD Operating Supply Current	VDD = 5.0V, no loading, 12 MHz		15		mA
I_{SB1}	Standby Current	Internal Oscillators, Bandgap, Flash, CPU Clock, Timer Clock, USB Clock all disabled			10	µA
USB Interface						
V_{ON}	Static Output High	15K ± 5% Ohm to VSS	2.8		3.6	V
V_{OFF}	Static Output Low	RUP is enabled			0.3	V
V_{DI}	Differential Input Sensitivity		0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2	V
C_{IN}	Transceiver Capacitance				20	pF
I_{IO}	Hi-Z State Data Line Leakage	0V < VIN < 3.3V	-10		10	mA

(Continued)

Parameter	Description General	Conditions	Min	Typ.	Max.	Unit
SPI / GPIO Interface						
R_{UP}	Pull up Resistance		4		12	KΩ
V_{ICR}	Input Threshold Voltage Low, CMOS mode	Low to High edge	40%		65%	VDD
V_{ICF}	Input Threshold Voltage Low, CMOS mode	High to Low edge	30%		55%	VDD
V_{ILTTL}	Input Low Voltage, TTL Mode	I/O-pin Supply = 2.9–3.6V			0.8	V
V_{IHTTL}	Input High Voltage, TTL Mode	I/O-pin Supply = 4.0–5.5V	2			V
V_{OL}	Output Low Voltage	IOL2 = 8 mA			0.4	V
V_{OH}	Output High Voltage	IOH = 2 mA	VDD – 0.5			V
C_{LOAD}	Maximum load capacitance				50	pF

7-3 AC Characteristics

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Driver						
T_{R1}	Transition Rise Time	CLOAD = 200 pF	75			ns
T_{R2}	Transition Rise Time	CLOAD = 600 pF			300	ns
T_{F1}	Transition Fall Time	CLOAD = 200 pF	75			ns
T_{F2}	Transition Fall Time	CLOAD = 600 pF			300	ns
T_R	Rise/Fall Time Matching		80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
USB Data Timing						
T_{DRATE}	Low-speed Data Rate	Ave. Bit Rate (1.5 Mbps ± 1.5%)	1.4775		1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	-75		75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	-45		45	ns
T_{DEOP}	Differential to EOP Transition Skew		-40		100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP			330	ns

(Continued)

Parameter	Description	Conditions	Min	Typ.	Max.	Unit

USB Data Timing						
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675			ns
T_{EOPT}	Source EOP Width		1.25		1.5	µs
T_{EOPT}	Source EOP Width		1.25		1.5	µs
T_{UDJ1}	Differential Driver Jitter	To next transition	-95		95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	-95		95	ns
T_{LST}	Width of SE0 during Diff. Transition				210	ns
SPI / GPIO Interface						
T_{R_SPI}	Output Rise Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			50	ns
T_{F_SPI}	Output Fall Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			15	ns

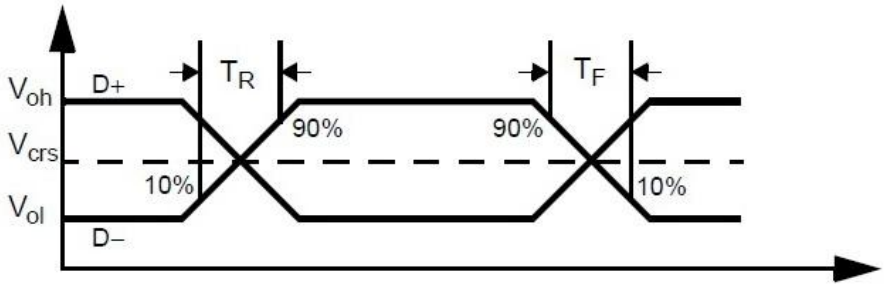

Figure 7-1 : USB Data Signal Timing

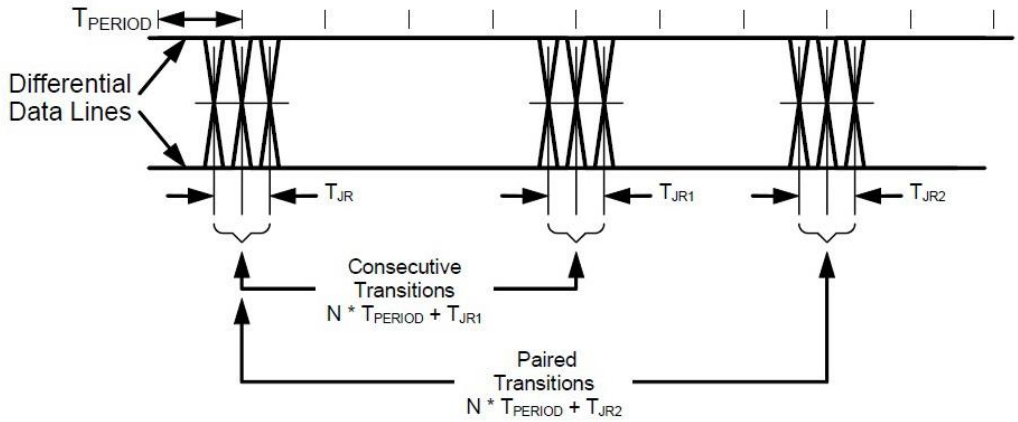

Figure 7-2 : Receiver Jitter Tolerance

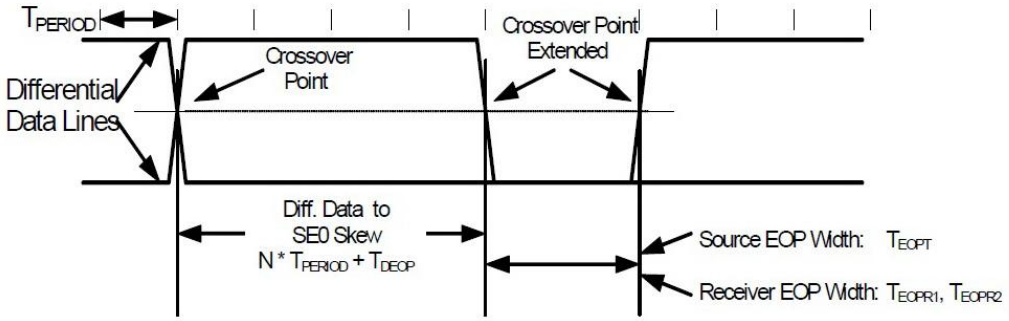

Figure 7-3 : Differential to EOP Transition Skew and EOP Width

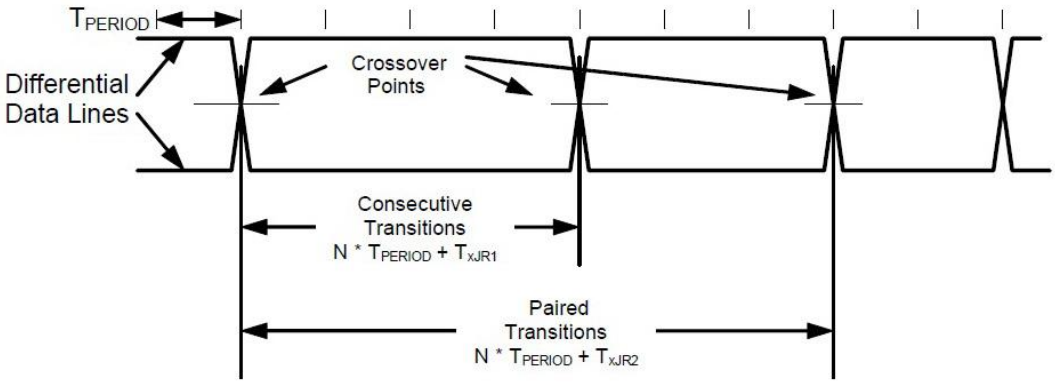

Figure 7-4 : Differential Data Jitter

8. Application Circuit

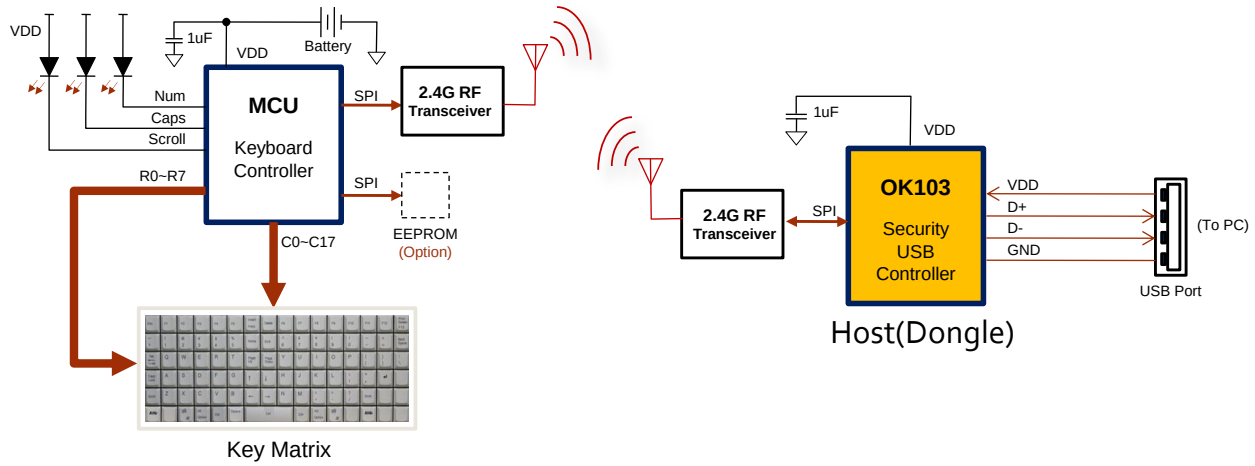

Figure 8-1 : Application Block Diagram

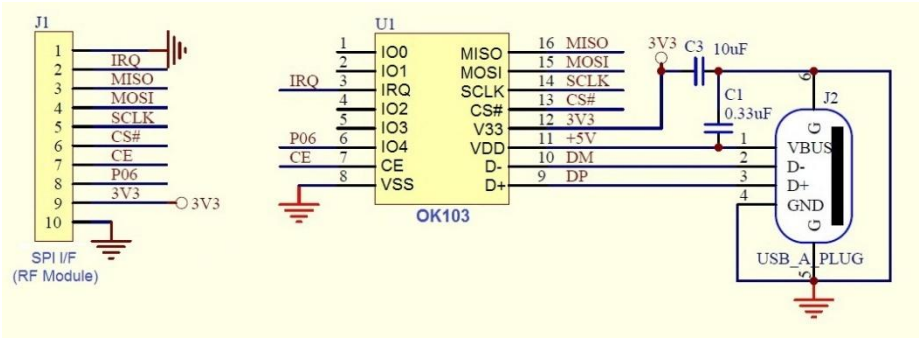

Figure 8-2 : Application Circuit

Figure 8-3 : Application Field