OK103

鍵盤加密控制器

規 格 書

Version 1.0

August 12, 2011

oTHE Technology Inc.

版 本 更 新 記 錄		
版 本	日 期	說 明
1.0	August 12, 2011	Preliminary version

Chapter Contents Page

1. 簡介

OK103 是一個用在 2.4G 無線鍵盤的加密控制器。其內部包含經美國 NIST FIPS 認證的 AES 加密引擎，透過 OK103 組合成的無線鍵盤與軟體端的加密整合技術，可以主動防治網路駭客或鍵盤側錄軟體等的惡意盜取個人資訊，解決使用者在上網時的疑慮，及被側錄的情況發生。

OK103 內含奧樂科技自行研發的 8-Bit MCU、加密運算器及 8K Bytes Flash，它提供 USB V2.0 的介面與 V1.1 的通訊協議，OK103 是一 SOIC-16Pin 的封裝，用在標準個人電腦的 2.4G RF 無線鍵盤的 Dongle 接收器(Host 端)，對鍵盤製造商而言，OK103 可以應用在現有的 2.4G RF 無線鍵盤，甚至不需要修改鍵盤本體(Device 端)的軟硬體及外觀，是一個同時可以做到低成本、高安全性與實用性的無線鍵盤加密保護方案。

2. 功能

- 內建 8-Bit MCU 及硬體加密運算器
- USB 2.0 界面 low speed 及 V1.1 協議
- 內建 256 Bytes SRAM 與 8KB Flash
- 內建 AES 加密引擎 (US NIST FIPS 認證 #1576)
- 提供 SPI 與 GPIO 介面
- 內建 3.3V 電壓調整器
- 內建 12 MHz 振盪器
- 3/5V I/O 內建提昇電阻
- 工作溫度: 0~70°C
- 供應電壓 : 4.5~5.5V
- 封裝: SOIC-16 pin

3. 內部方塊圖

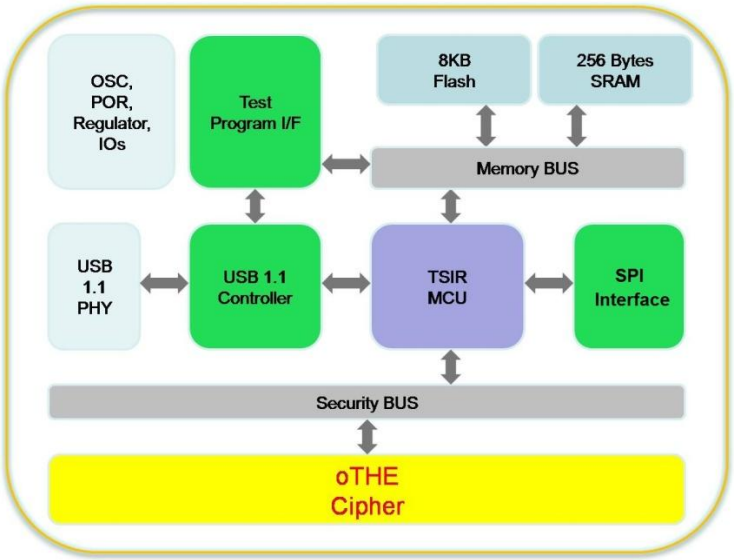

圖 3-1：內部方塊圖

4. 腳位圖

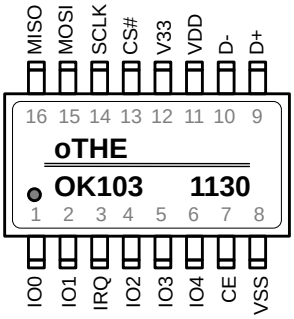

圖 4-1 : 腳位圖

5. 腳位定義

表 5-1 : 腳位定義

Pin No.	腳 位 名 稱	說　　明	Pin state
1,2,4,5,6	IO[4:0]	General Purpose I/O Pins	Bi-direction
3	IRQ	Interrupt request pin.	Input
7	CE	Chip Enable Activates RX or TX mode	Output
8	VSS	Power Ground	Power
9	D-	USB I/F D-	USB PHY
10	D+	USB I/F D+	USB PHY
11	VDD	Power Supply	Power
12	V33	Regulator Output	Power
13	CS#	SPI Chip Select	Output
14	SCLK	SPI Clock	Output
15	MOSI	SPI Data Output	Output
16	MISO	SPI Data Input	Input

6. 封裝

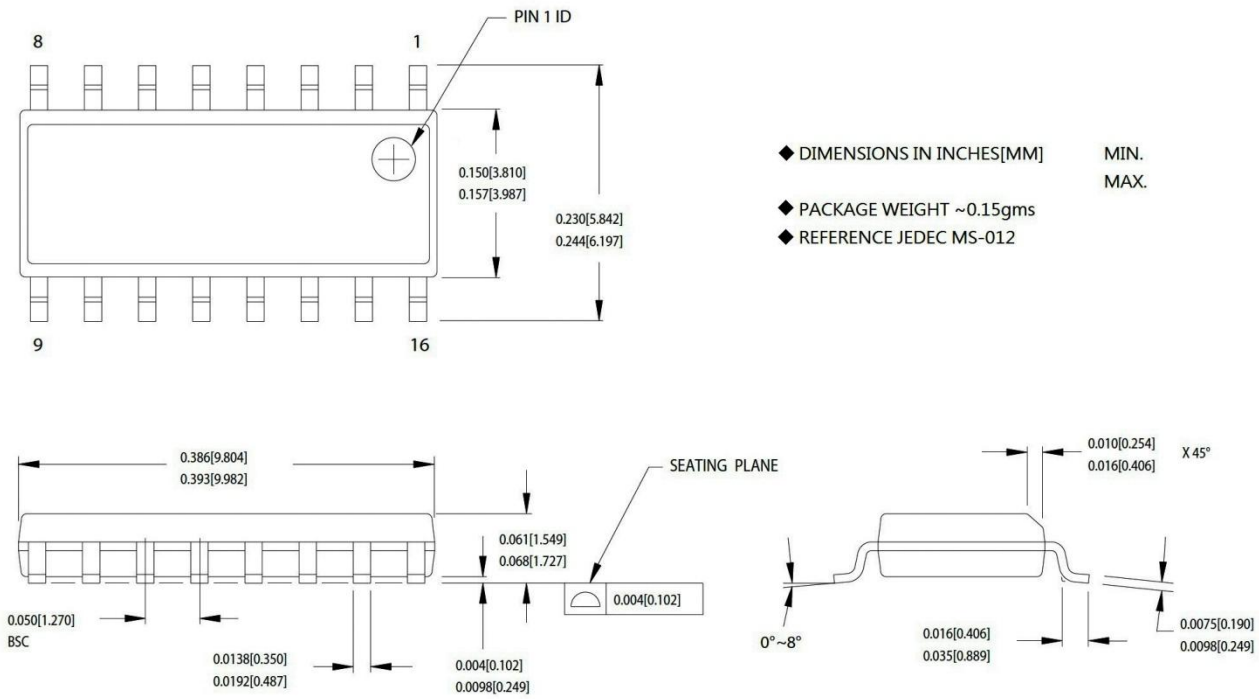

圖 6-1 : 16-Lead (150-Mil) SOIC

7. 電氣特性

7-1 最大極限

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –0°C to +70°C

Supply Voltage on VDD Relative to VSS..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to + VCC + 0.5V

DC Voltage Applied to Outputs in High-Z State ..... –0.5V to + VCC + 0.5V

Power Dissipation ..... 300 mW

Static Discharge Voltage 2200V

Latch-up Current ..... 200 mA

7-2 DC 特性

表 7-1 : DC 特性

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
	General					
V_{DD}	Operating Voltage	USB activity, 12 MHz	4.35		5.25	V
V_{33}	Regulator Voltage	USB activity, 12 MHz		3.3		V
T_{FP}	Operating Temp	Flash Programming	0		70	°C
I_{CC2}	VDD Operating Supply Current	VDD = 5.0V, no loading, 12 MHz		15		mA
I_{SB1}	Standby Current	Internal Oscillators, Bandgap, Flash, CPU Clock, Timer Clock, USB Clock all disabled			10	µA
USB Interface						
V_{ON}	Static Output High	15K ± 5% Ohm to VSS	2.8		3.6	V
V_{OFF}	Static Output Low	RUP is enabled			0.3	V
V_{DI}	Differential Input Sensitivity		0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2	V
C_{IN}	Transceiver Capacitance				20	pF
I_{IO}	Hi-Z State Data Line Leakage	0V < VIN < 3.3V	-10		10	mA

(Continued)

Parameter	Description General	Conditions	Min	Typ.	Max.	Unit
SPI / GPIO Interface						
R_{UP}	Pull up Resistance		4		12	KΩ
V_{ICR}	Input Threshold Voltage Low, CMOS mode	Low to High edge	40%		65%	VDD
V_{ICF}	Input Threshold Voltage Low, CMOS mode	High to Low edge	30%		55%	VDD
V_{ILTTL}	Input Low Voltage, TTL Mode	I/O-pin Supply = 2.9–3.6V			0.8	V
V_{IHTTL}	Input High Voltage, TTL Mode	I/O-pin Supply = 4.0–5.5V	2			V
V_{OL}	Output Low Voltage	IOL2 = 8 mA			0.4	V
V_{OH}	Output High Voltage	IOH = 2 mA	VDD – 0.5			V
C_{LOAD}	Maximum load capacitance				50	pF

7-3 AC 特性

表 7-2：AC 特性

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Driver						
T_{R1}	Transition Rise Time	CLOAD = 200 pF	75			ns
T_{R2}	Transition Rise Time	CLOAD = 600 pF			300	ns
T_{F1}	Transition Fall Time	CLOAD = 200 pF	75			ns
T_{F2}	Transition Fall Time	CLOAD = 600 pF			300	ns
T_R	Rise/Fall Time Matching		80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
USB Data Timing						
T_{DRATE}	Low-speed Data Rate	Ave. Bit Rate (1.5 Mbps ± 1.5%)	1.4775		1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	-75		75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	-45		45	ns
T_{DEOP}	Differential to EOP Transition Skew		-40		100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP			330	ns
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675			ns
T_{EOPT}	Source EOP Width		1.25		1.5	μs
T_{EOPT}	Source EOP Width		1.25		1.5	μs
T_{UDJ1}	Differential Driver Jitter	To next transition	-95		95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	-95		95	ns
T_{LST}	Width of SE0 during Diff. Transition				210	ns
SPI / GPIO Interface						
T_{R_SPI}	Output Rise Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			50	ns
T_{F_SPI}	Output Fall Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			15	ns

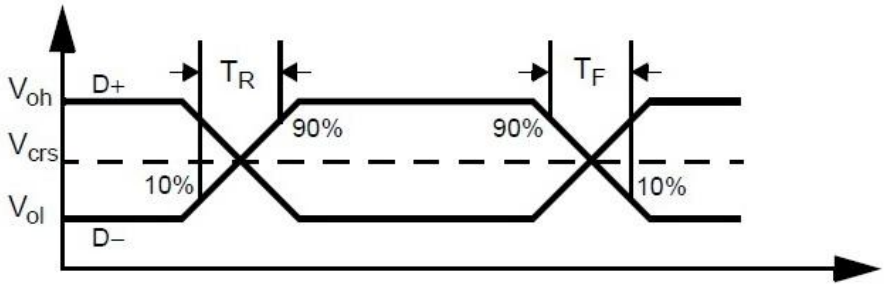

圖 7-1 : USB Data Signal Timing

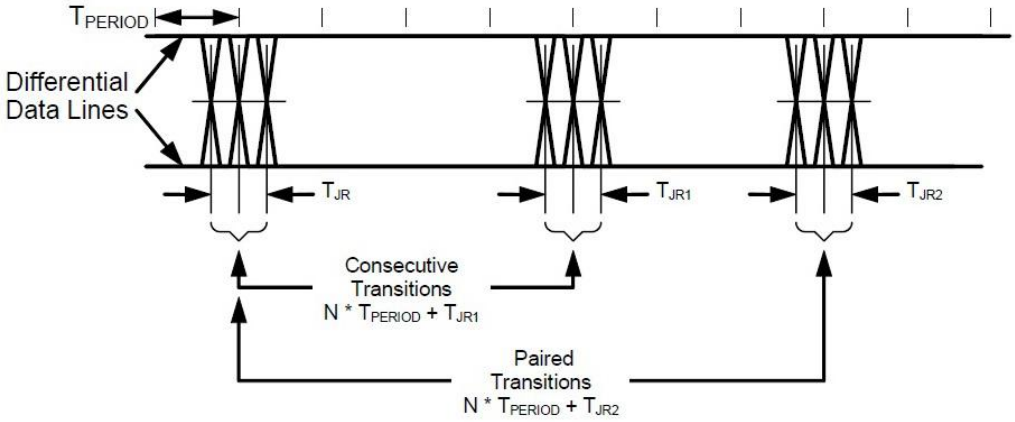

圖 7-2 : Receiver Jitter Tolerance

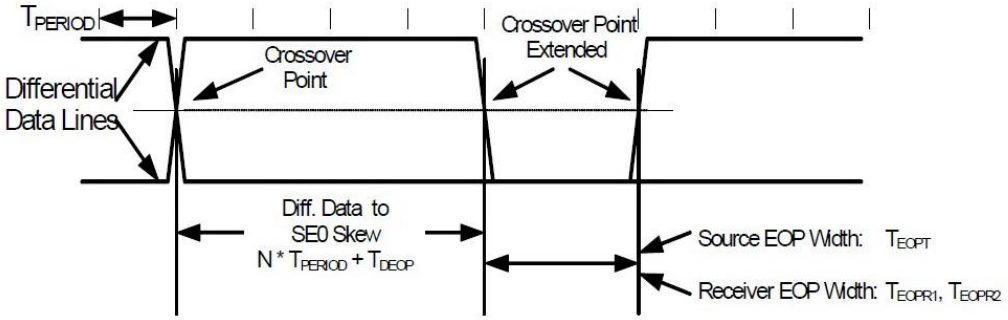

圖 7-3 : Differential to EOP Transition Skew and EOP Width

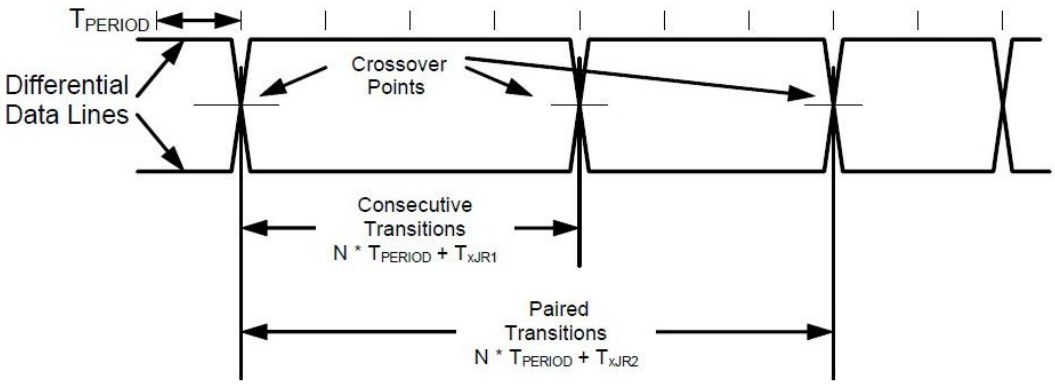

圖 7-4 : Differential Data Jitter

8. 應用電路

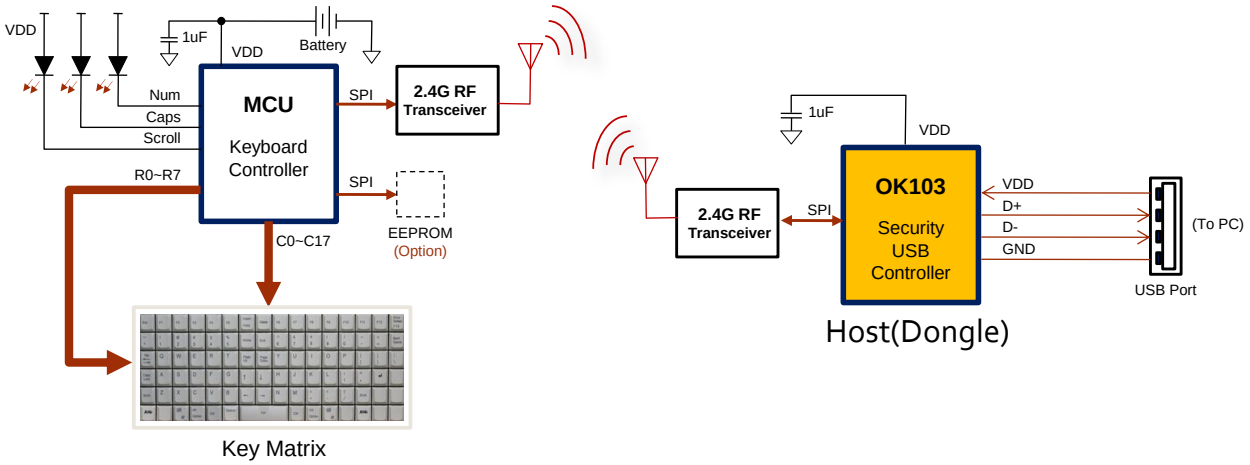

圖 8-1：應用電路方塊圖

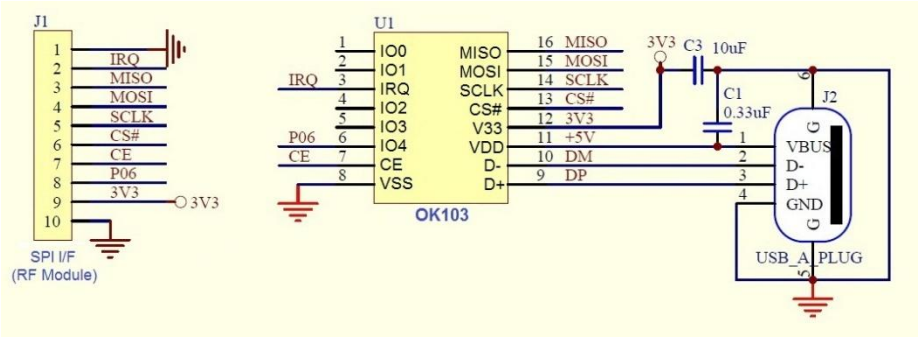

圖 8-2：應用電路方塊圖

圖 8-3：應用領域