OK100

Keyboard Security Controller

Specification

Version 1.0

October 12, 2010

oTHE Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	October 12, 2010	Preliminary version

Chapter Contents Page

1. Introduction

OK100 is a keyboard security controller. It contains 8-Bit MCU, encryption calculator, 8K Bytes Flash, SRAM, USB 1.1 controller and PS2 controller circuit. OK100 and software through the integration of encryption technology, can take the initiative to prevention network hackers or other malicious software(Keylogger) to steal personal information. OK100 is a SOIC-16Pin package can be built within the PC keyboard, made USB/PS2 Adapter, or built within the motherboard. It can be resolved when the user concerns in the Internet, and was be-logged happens. It is a low-cost, high security encryption and practical solutions.

2. Features

- Embedded 8bit MCU and H/W Encrypter
- USB 2.0 Interface
- Embedded RAM 256 Bytes
- Embedded Flash 8KB
- Internal 12 MHz Oscillator
- 3/5V I/O with Pull-up Resistor
- Operating Temperature: 0~70°C
- Operating Voltage : 4.5~5.5V
- Package: SOIC-16 pin

3. Pin Assignment

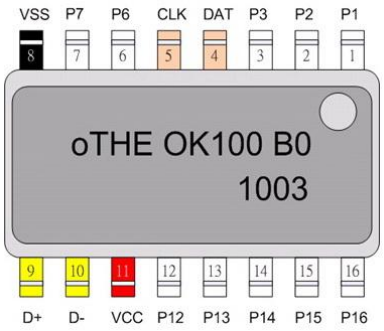

Figure 3-1 : Pin Assignment

4. Pin Definition

Pin No.	Pin Name	Description	Pin state	Reset State
4	*DAT*	*PS2 Device Interface data*	*Open drain*	HiZ / HiZ
5	*CLK*	*PS2 Device Interface clock*	*Open drain*	HiZ / HiZ
8	*D+*	*USB I/F D+*	*USB PHY*	HiZ / HiZ
9	*D-*	*USB I/F D-*	*USB PHY*	HiZ / HiZ
10	*VSS*	*Power Ground*	*Power*	
11	*VCC*	*Power VCC*	*Power*	
others	*P[16:1]*	*Test Pins*	*Input pull up*	HiZ / HiZ

5. Internal Block Diagram

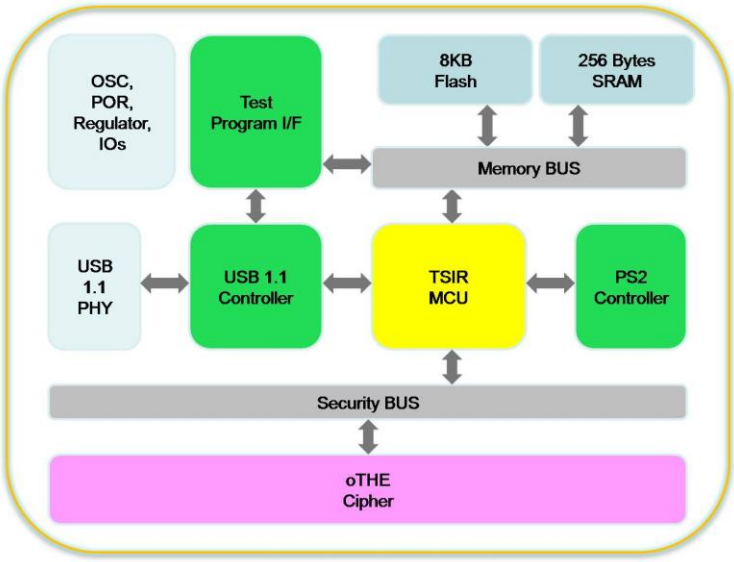

Figure 5-1 : Internal Block Diagram

6. Package(SOIC-16Pin)

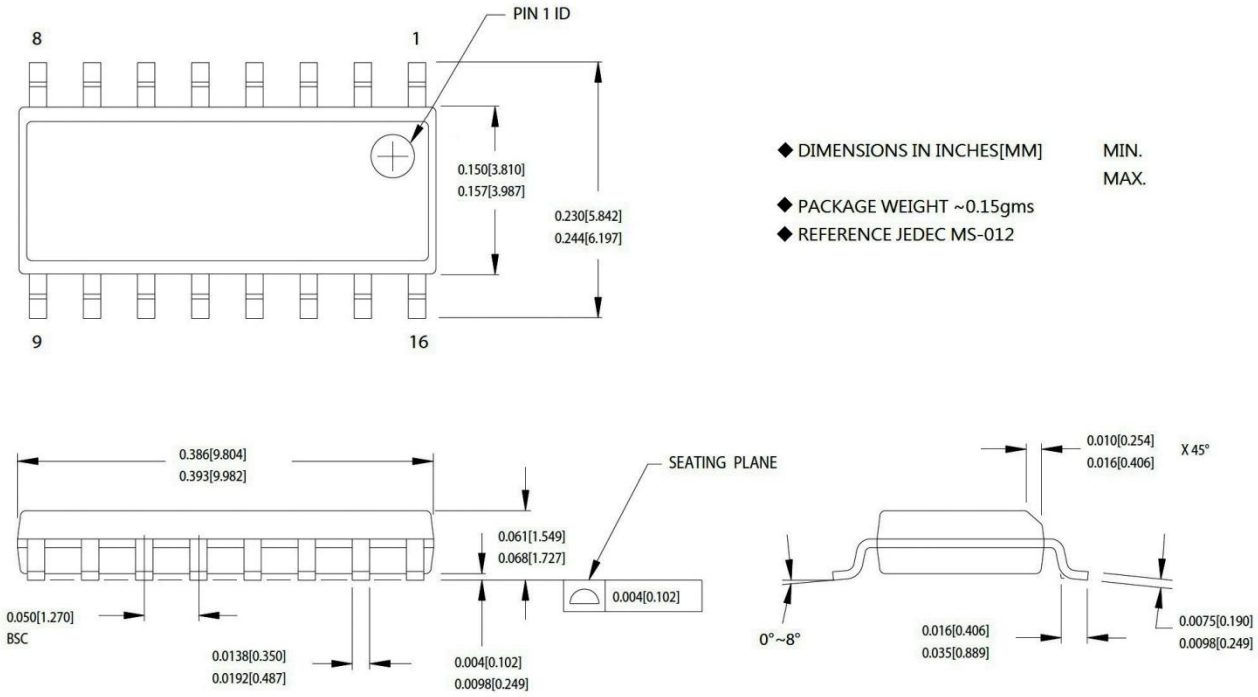

Figure 6-1 : 16-Lead (150-Mil) SOIC

7. Electrical Characteristics

7-1 Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
Supply Voltage on VCC Relative to VSS	–0.5V to +7.0V
DC Input Voltage	–0.5V to + VCC + 0.5V
DC Voltage Applied to Outputs in High-Z State	–0.5V to + VCC + 0.5V
Power Dissipation	300 mW
Static Discharge Voltage	2200V
Latch-up Current	200 mA

7-2 DC Characteristics

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
	General					
V_{CC1}	Operating Voltage	No USB activity, 12 MHz	4.2		5.5	V
V_{CC2}	Operating Voltage	USB activity, 12 MHz	4.35		5.25	V
T_{FP}	Operating Temp	Flash Programming	0		70	°C
I_{CC1}	VCC Operating Supply Current	VCC = 5.25V, no loading, 12 MHz			30	mA
I_{CC2}	VCC Operating Supply Current	VCC = 5.0V, no loading, 12 MHz		15		mA
I_{SB1}	Standby Current	Internal Oscillators, Bandgap, Flash, CPU Clock, Timer Clock, USB Clock all disabled			10	µA
USB Interface						
V_{ON}	Static Output High	15K ± 5% Ohm to VSS	2.8		3.6	V
V_{OFF}	Static Output Low	RUP is enabled			0.3	V
V_{DI}	Differential Input Sensitivity		0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2	V
C_{IN}	Transceiver Capacitance				20	pF
I_{IO}	Hi-Z State Data Line Leakage	0V < VIN < 3.3V	-10		10	mA

(Continued)

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
	General					
PS2 Device Interface						
R_{UP}	Pull up Resistance		4		12	KΩ
V_{ICR}	Input Threshold Voltage Low, CMOS mode	Low to High edge	40%		65%	VCC
V_{ICF}	Input Threshold Voltage Low, CMOS mode	High to Low edge	30%		55%	VCC
V_{ILTTL}	Input Low Voltage, TTL Mode	I/O-pin Supply = 2.9–3.6V			0.8	V
V_{IHTTL}	Input High Voltage, TTL Mode	I/O-pin Supply = 4.0–5.5V	2			V
V_{OL}	Output Low Voltage	IOL2 = 8 mA			0.4	V
V_{OH}	Output High Voltage	IOH = 2 mA	VCC – 0.5			V
C_{LOAD}	Maximum load capacitance				50	pF

7-3 AC Characteristics

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Driver						
T_{R1}	Transition Rise Time	CLOAD = 200 pF	75			ns
T_{R2}	Transition Rise Time	CLOAD = 600 pF			300	ns
T_{F1}	Transition Fall Time	CLOAD = 200 pF	75			ns
T_{F2}	Transition Fall Time	CLOAD = 600 pF			300	ns
T_R	Rise/Fall Time Matching		80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
USB Data Timing						
T_{DRATE}	Low-speed Data Rate	Ave. Bit Rate (1.5 Mbps ± 1.5%)	1.4775		1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	-75		75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	-45		45	ns
T_{DEOP}	Differential to EOP Transition Skew		-40		100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP			330	ns

(Continued)

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Data Timing						
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675			ns
T_{EOPT}	Source EOP Width		1.25		1.5	µs
T_{EOPT}	Source EOP Width		1.25		1.5	µs
T_{UDJ1}	Differential Driver Jitter	To next transition	-95		95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	-95		95	ns
T_{LST}	Width of SE0 during Diff. Transition				210	ns
PS2 Device Interface						
T_{R_CLK} T_{R_DAT}	Output Rise Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			50	ns
T_{F_CLK} T_{R_DAT}	Output Fall Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			15	ns

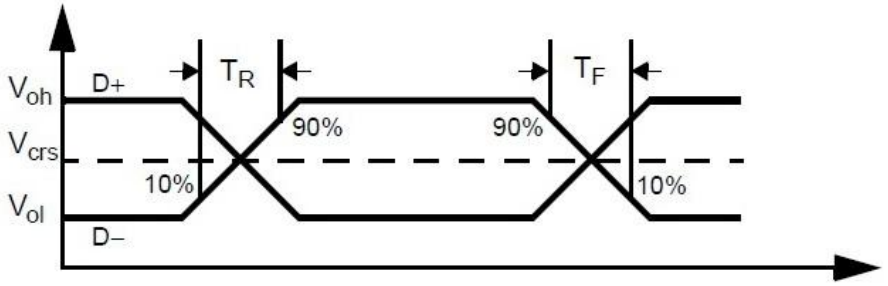

Figure 7-1 : USB Data Signal Timing

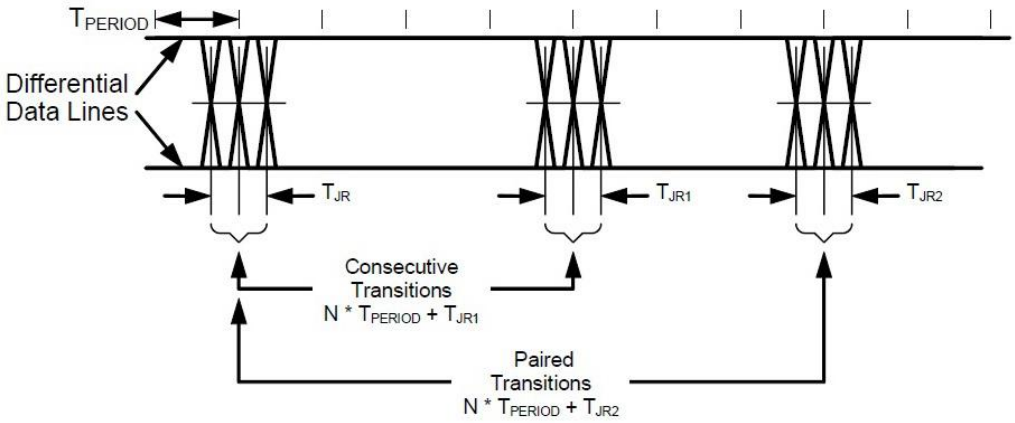

Figure 7-2 : Receiver Jitter Tolerance

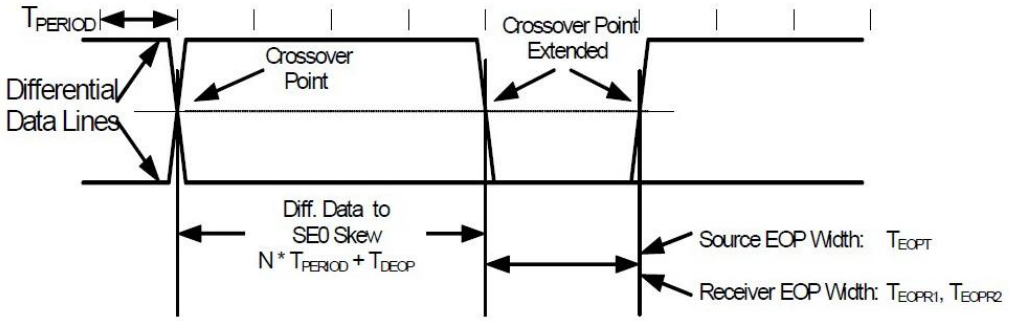

Figure 7-3 : Differential to EOP Transition Skew and EOP Width

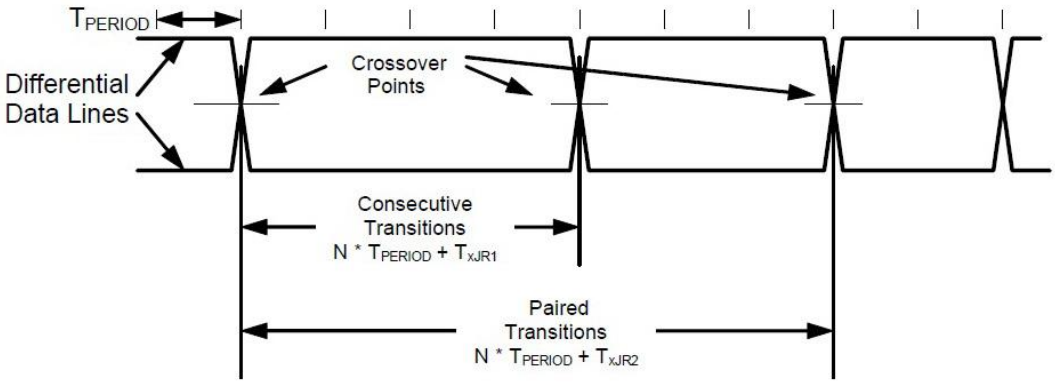

Figure 7-4 : Differential Data Jitter

8. Application Circuit

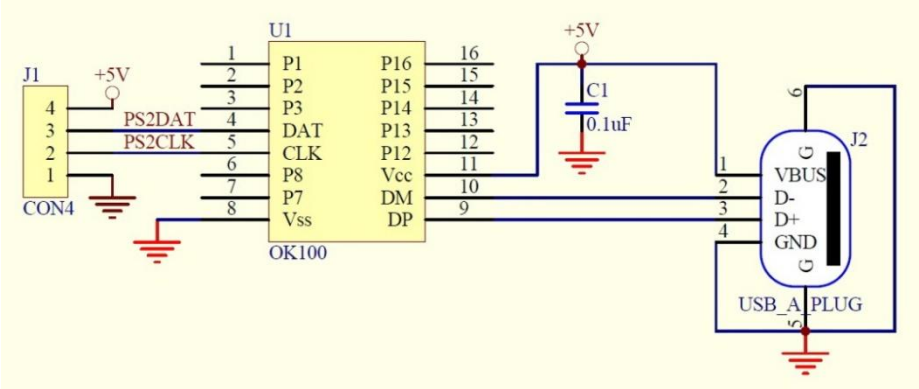

Figure 8-1 : Application Circuit

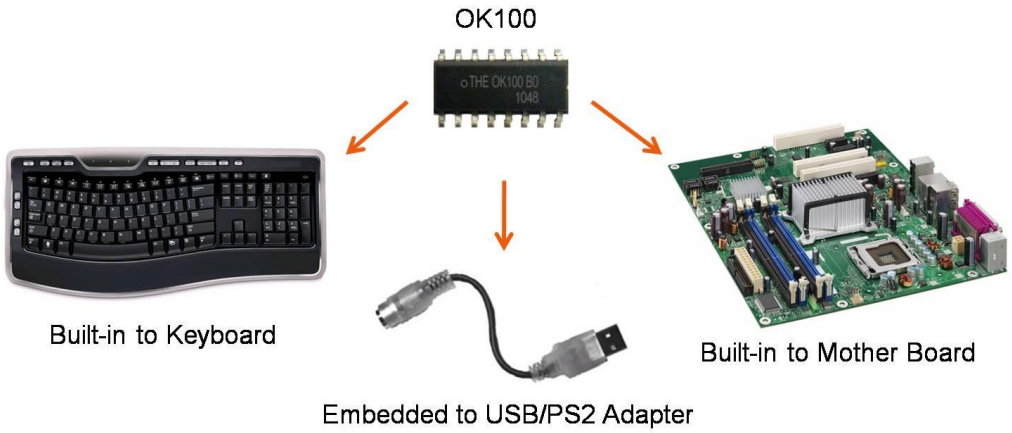

Figure 8-2 : Application Fields