OK100

鍵盤加密控制器

規 格 書

Version 1.0

October 12, 2010

oTHE Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	October 12, 2010	Preliminary version

Chapter Contents Page

1. 簡介

OK100 是一鍵盤加密控制器。內含 8-Bit MCU、加密運算器、8K Bytes Flash、SRAM、USB 1.1 控制器、PS2 控制器等電路。透過 OK100 與軟體端的加密整合技術，可以主動防治網路駭客或鍵盤側錄軟體等的惡意盜取個人資訊。OK100 是一 SOIC-16Pin 的封裝，可內建在 PC 鍵盤內、做成 USB/PS2 Adapter，或是內建在主機板內，解決使用者在上網時的疑慮，及被側錄的情況發生，是一個同時可以做到低成本、高安全性與實用性的加密保護方案。

2. 功能

- 內建 8-Bit MCU 及加密運算器
- USB 2.0 界面
- 內建 RAM 256 Bytes
- 內建 Flash 8KB
- 內建 12 MHz 振盪器
- 3/5V I/O 內建提昇電阻
- 工作溫度: 0~70°C
- 供應電壓 : 4.5~5.5V
- 封裝: SOIC-16 pin

3. 腳位圖

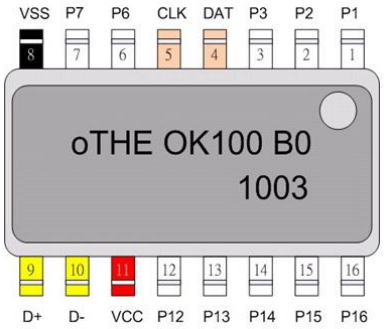

圖 3-1 : 腳位圖

4. 腳位定義

Pin No.	腳 位 名 稱	說　　明	Pin state	Reset State
4	*DAT*	*PS2 Device Interface data*	*Open drain*	HiZ / HiZ
5	*CLK*	*PS2 Device Interface clock*	*Open drain*	HiZ / HiZ
8	*D+*	*USB I/F D+*	*USB PHY*	HiZ / HiZ
9	*D-*	*USB I/F D-*	*USB PHY*	HiZ / HiZ
10	*VSS*	*Power Ground*	*Power*	
11	*VCC*	*Power VCC*	*Power*	
others	*P[16:1]*	*Test Pins*	*Input pull up*	HiZ / HiZ

5. 內部方塊圖

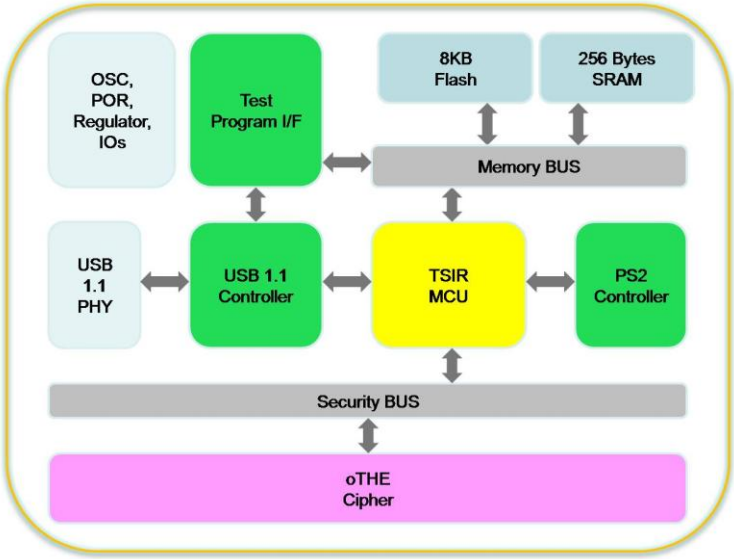

圖 5-1：內部方塊圖

6. 封裝(SOIC-16Pin)

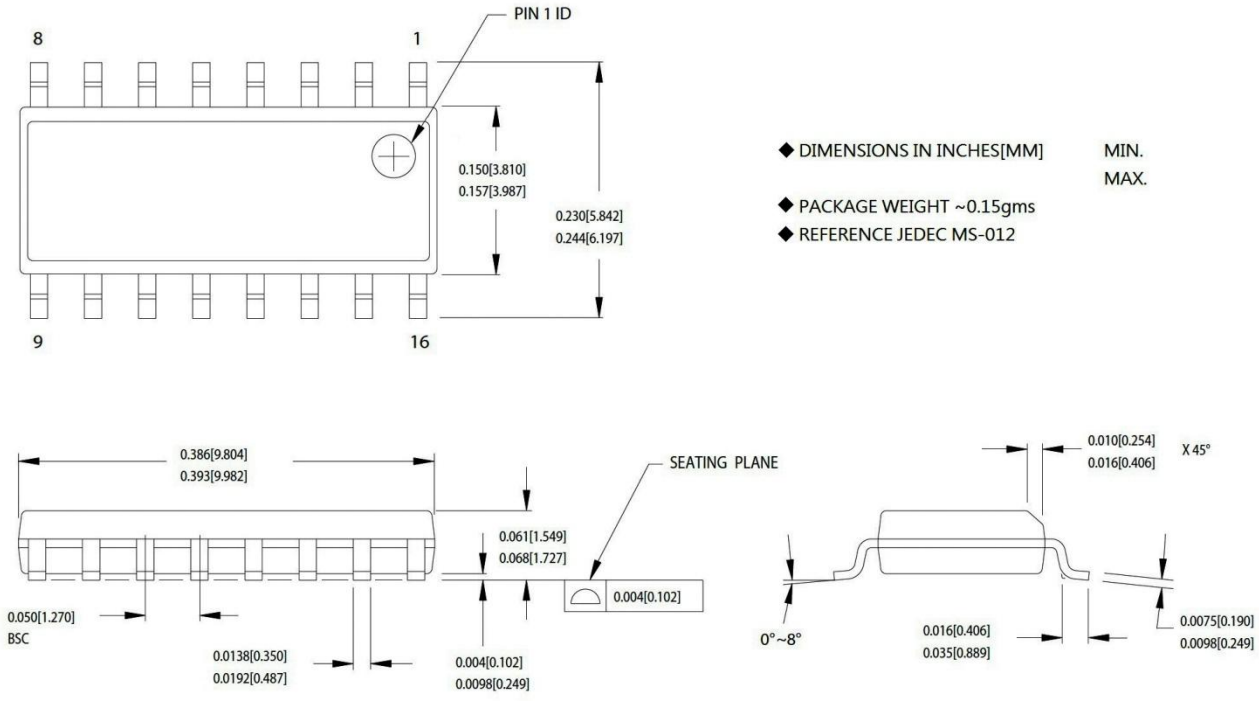

圖 6-1：16-Lead (150-Mil) SOIC

7. 電氣特性

7-1 最大極限

Storage Temperature ..... –65°C to +150°C
Ambient Temperature with Power Applied ..... –0°C to +70°C
Supply Voltage on VCC Relative to VSS..... –0.5V to +7.0V
DC Input Voltage ..... –0.5V to + VCC + 0.5V
DC Voltage Applied to Outputs in High-Z State ..... –0.5V to + VCC + 0.5V
Power Dissipation ..... 300 mW
Static Discharge Voltage 2200V
Latch-up Current ..... 200 mA

7-2 DC 特性

Parameter	Description General	Conditions	Min	Typ.	Max.	Unit
V_{CC1}	Operating Voltage	No USB activity, 12 MHz	4.2		5.5	V
V_{CC2}	Operating Voltage	USB activity, 12 MHz	4.35		5.25	V
T_{FP}	Operating Temp	Flash Programming	0		70	°C
I_{CC1}	VCC Operating Supply Current	VCC = 5.25V, no loading, 12 MHz			30	mA
I_{CC2}	VCC Operating Supply Current	VCC = 5.0V, no loading, 12 MHz		15		mA
I_{SB1}	Standby Current	Internal Oscillators, Bandgap, Flash, CPU Clock, Timer Clock, USB Clock all disabled			10	µA
USB Interface						
V_{ON}	Static Output High	15K ± 5% Ohm to VSS	2.8		3.6	V
V_{OFF}	Static Output Low	RUP is enabled			0.3	V
V_{DI}	Differential Input Sensitivity		0.2			V
V_{CM}	Differential Input Common Mode Range		0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8		2	V
C_{IN}	Transceiver Capacitance				20	pF
I_{IO}	Hi-Z State Data Line Leakage	0V < VIN < 3.3V	-10		10	mA

(Continued)

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
	General					
PS2 Device Interface						
R_{UP}	Pull up Resistance		4		12	KΩ
V_{ICR}	Input Threshold Voltage Low, CMOS mode	Low to High edge	40%		65%	VCC
V_{ICF}	Input Threshold Voltage Low, CMOS mode	High to Low edge	30%		55%	VCC
V_{ILTTL}	Input Low Voltage, TTL Mode	I/O-pin Supply = 2.9–3.6V			0.8	V
V_{IHTTL}	Input High Voltage, TTL Mode	I/O-pin Supply = 4.0–5.5V	2			V
V_{OL}	Output Low Voltage	IOL2 = 8 mA			0.4	V
V_{OH}	Output High Voltage	IOH = 2 mA	VCC – 0.5			V
C_{LOAD}	Maximum load capacitance				50	pF

7-3 AC 特性

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Driver						
T_{R1}	Transition Rise Time	CLOAD = 200 pF	75			ns
T_{R2}	Transition Rise Time	CLOAD = 600 pF			300	ns
T_{F1}	Transition Fall Time	CLOAD = 200 pF	75			ns
T_{F2}	Transition Fall Time	CLOAD = 600 pF			300	ns
T_R	Rise/Fall Time Matching		80		125	%
V_{CRS}	Output Signal Crossover Voltage		1.3		2.0	V
USB Data Timing						
T_{DRATE}	Low-speed Data Rate	Ave. Bit Rate (1.5 Mbps ± 1.5%)	1.4775		1.5225	Mbps
T_{DJR1}	Receiver Data Jitter Tolerance	To next transition	-75		75	ns
T_{DJR2}	Receiver Data Jitter Tolerance	To pair transition	-45		45	ns
T_{DEOP}	Differential to EOP Transition Skew		-40		100	ns
T_{EOPR1}	EOP Width at Receiver	Rejects as EOP			330	ns

(Continued)

Parameter	Description	Conditions	Min	Typ.	Max.	Unit
USB Data Timing						
T_{EOPR2}	EOP Width at Receiver	Accept as EOP	675			ns
T_{EOPT}	Source EOP Width		1.25		1.5	µs
T_{EOPT}	Source EOP Width		1.25		1.5	µs
T_{UDJ1}	Differential Driver Jitter	To next transition	-95		95	ns
T_{UDJ2}	Differential Driver Jitter	To pair transition	-95		95	ns
T_{LST}	Width of SE0 during Diff. Transition				210	ns
PS2 Device Interface						
T_{R_CLK} T_{R_DAT}	Output Rise Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			50	ns
T_{F_CLK} T_{R_DAT}	Output Fall Time	Measured between 10 and 90% Vdd/Vreg with 50 pF load			15	ns

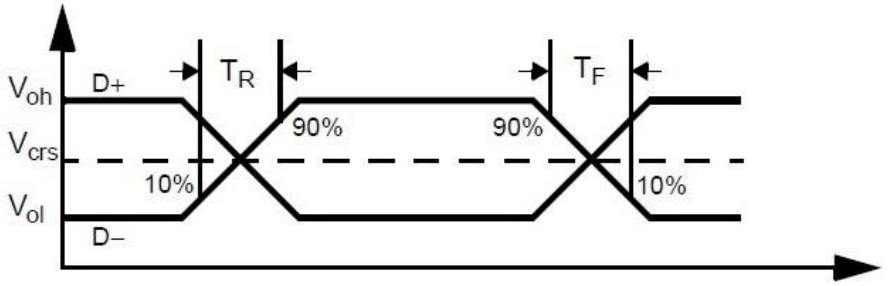

圖 7-1 : USB Data Signal Timing

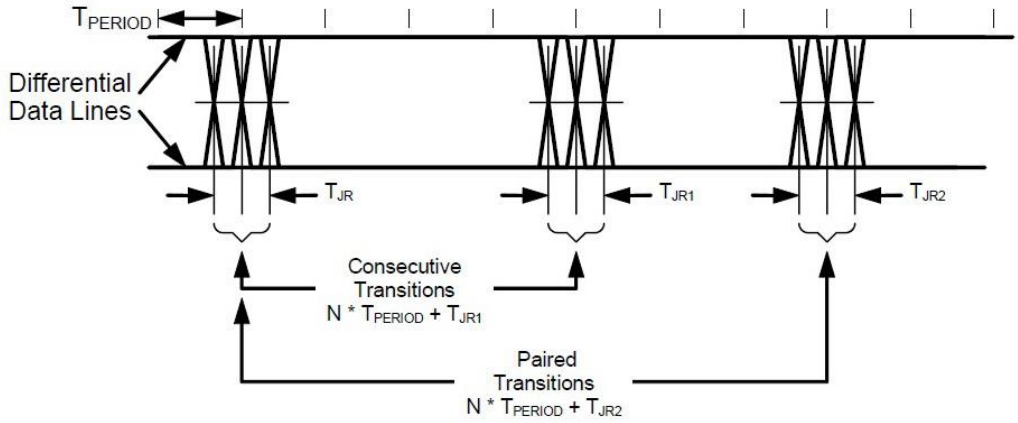

圖 7-2 : Receiver Jitter Tolerance

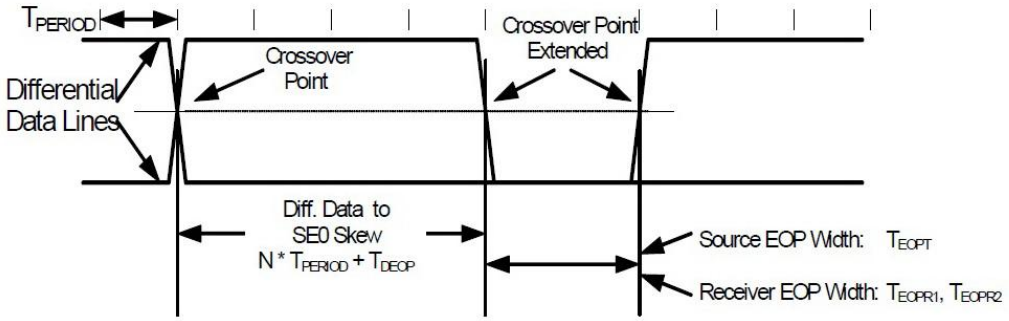

圖 7-3 : Differential to EOP Transition Skew and EOP Width

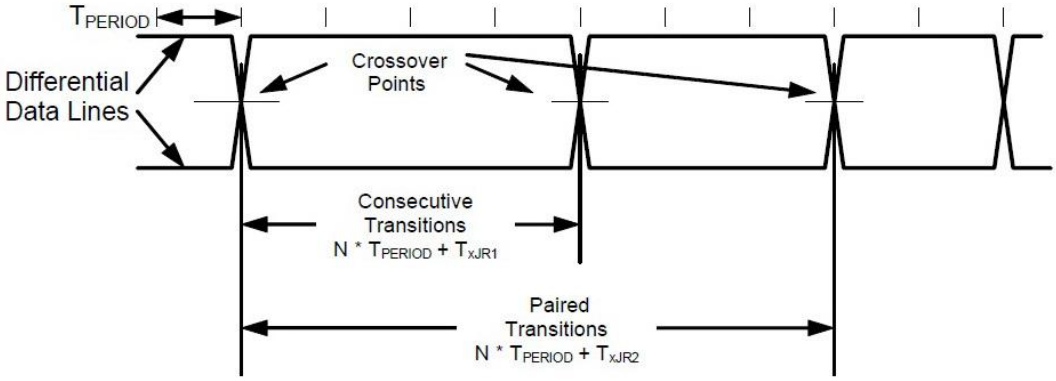

圖 7-4 : Differential Data Jitter

8. 應用電路

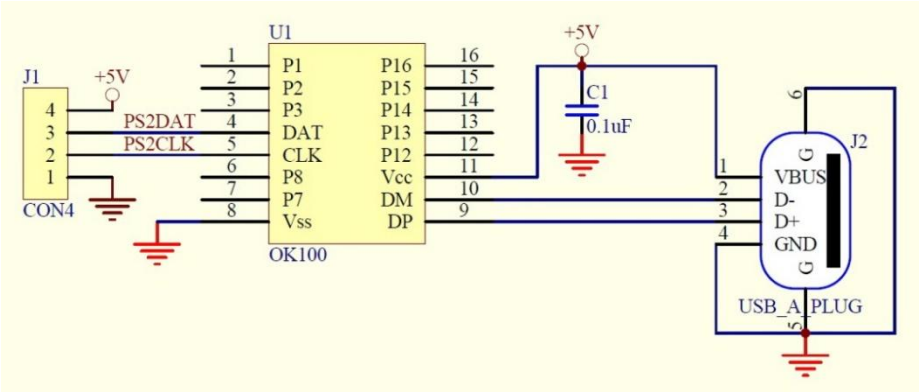

圖 8-1：應用電路

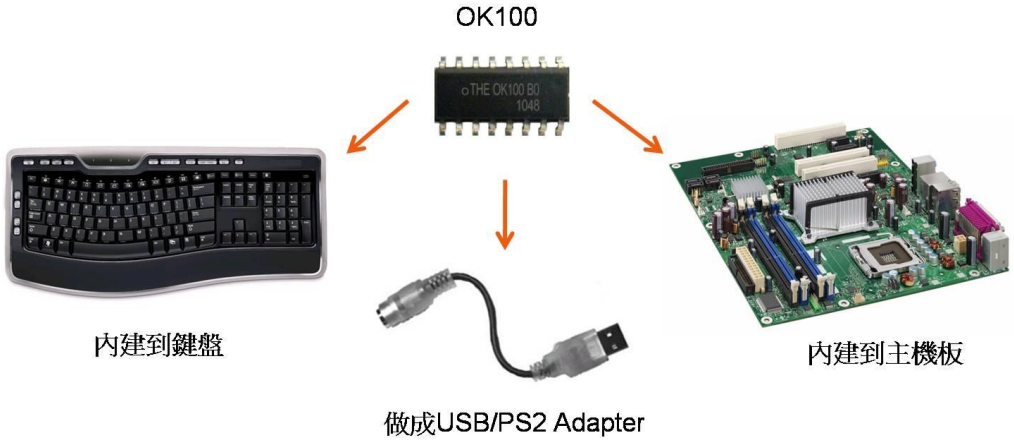

圖 8-2：應用領域